

Serial Peripheral Interface (SPI) Flash Memory: Multiple I/Os Bring High Performance to Low-Cost Memory Subsystems



THE CHALLENGE

As the demand to lower bill of materials costs continues to rise, the need for lower cost memory subsystems becomes more pressing. To date, manufacturers have used several tactics to reduce the cost of memory, including shrinking the die size, minimizing feature sets, and reducing the pin count from parallel to multiplexed address and data pins. Unfortunately, these approaches are still inadequate to satisfy the increasing demand to lower the cost of the memory subsystem in electronic designs. With the availability of serial peripheral interface (SPI) Flash memory, designers have a new opportunity to simplify memory subsystems and in turn reduce the cost of their design.

A LOW COST MEMORY SOLUTION

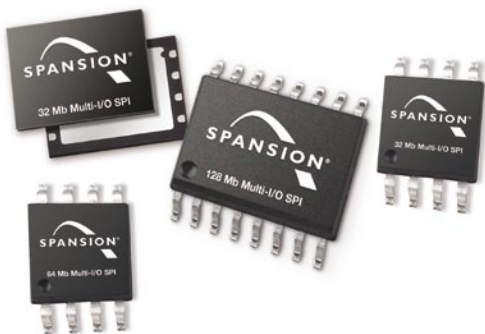
In order to contribute appreciably to lowering overall systems costs, manufacturers must look past just the component to the entire system. As memory manufacturers continue to innovate and create smaller die sizes and smaller packages, only by lowering pin count can you start to affect the memory subsystem. For this reason, serial Flash memory is an attractive solution for a variety of applications. The serial interface offers several benefits over the parallel interface in reducing overall systems costs including microcontroller and chipset pin-count reduction, smaller and simpler printed circuit boards, and lower power consumption. As a result, serial Flash memory unit volume has grown by more than 400 percent since 2004 and has represented almost 50 percent of the low-density (1-megabit (Mb) to 16 Mb) NOR Flash market.

Because of the lowest pin count, lowest package costs, and optimized testing capability, the unit cost for SPI Flash memory is the lowest amongst the alternative Flash memories at similar densities which translates into lower system costs for end applications.

With only eight pads, minimal die size can be achieved. In comparison, a x16 data bus based, 64 Mb parallel NOR Flash memory in ADM form (Address and Data Multiplexed), requires 33 pins (25 pins for address/data and eight control pins).

SOIC-8 and SOIC-16 are the lowest cost packages in the industry for eight or 16 pin lead-frame based solutions, and compared to a standard BGA package for conventional parallel NOR products, SPI packaging cost for a 8-pin SOIC is up to 70% less.

Low pin count leads to increased parallelization during testing which further lowers component costs by enabling the testing of a greater number of devices simultaneously on one tester compared to conventional parallel interface Flash memory devices.



The MirrorBit® SPI Multi-I/O family (32 Mb - 128 Mb) is the latest innovation from Spansion. By combining high read performance of up to 40 MB/s with the simplicity of the serial interface, designers have a new opportunity to reduce costs while maintaining application performance.

A NEW GENERATION OF PERFORMANCE

For design engineers, the move to reduce costs sometimes comes at the price of reduced performance. For applications that have switched from the parallel interface to standard serial interface, read performance of the memory declines by 50% to 70% (typical 90ns parallel Flash memory in byte or word mode, compared to the SPI Flash memory running at 50MHz in single I/O mode). The next generation of MirrorBit® SPI Flash memory is the Multiple I/O family. Multi I/O Flash memories will play an important role in expanding the applicability of SPI Flash memory to a broader array of applications due to its increased performance, while maintaining the lower cost benefits of the serial interface.

A multi I/O SPI device is capable of supporting increased bandwidth or throughput from a single device. A dual I/O (two-bit data bus) interface enables transfer rates to double compared to the standard serial Flash memory devices, while a quad I/O (four-bit data bus) interface improves throughput four times and opens up a much wider range of applications that require higher performance. Figure 1 shows the multi I/O SPI interconnection of a typical quad I/O serial hardware interface and how two such devices can be used in a system.

FIGURE 1: QUAD I/O SERIAL INTERCONNECTION

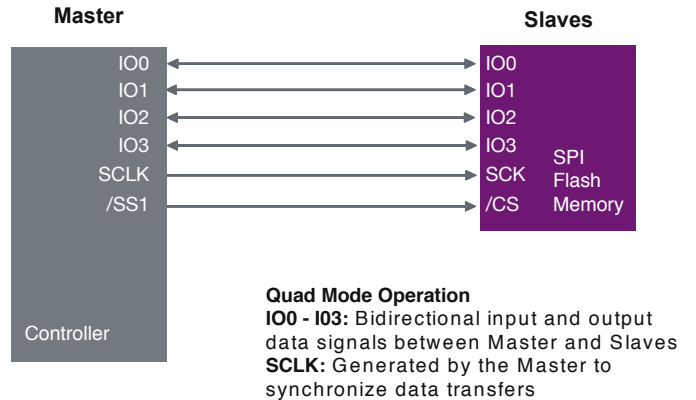


TABLE 1: THROUGHPUT COMPARISON BETWEEN SERIAL AND PARALLEL NOR

INTERFACE	MODE	ACCESS TIME (NS)	CLOCK (MHZ)	EFFECTIVE THROUGHPUT (MB/S)	TIME TO READ 32 MB OF DATA (MS)
PARALLEL	BYTE	90	11	11	377
	WORD	90	11	22	189
SERIAL	SINGLE I/O	12.5	104	13	323
	DUAL I/O	12.5	80	20	210
	QUAD I/O	12.5	80	40	105

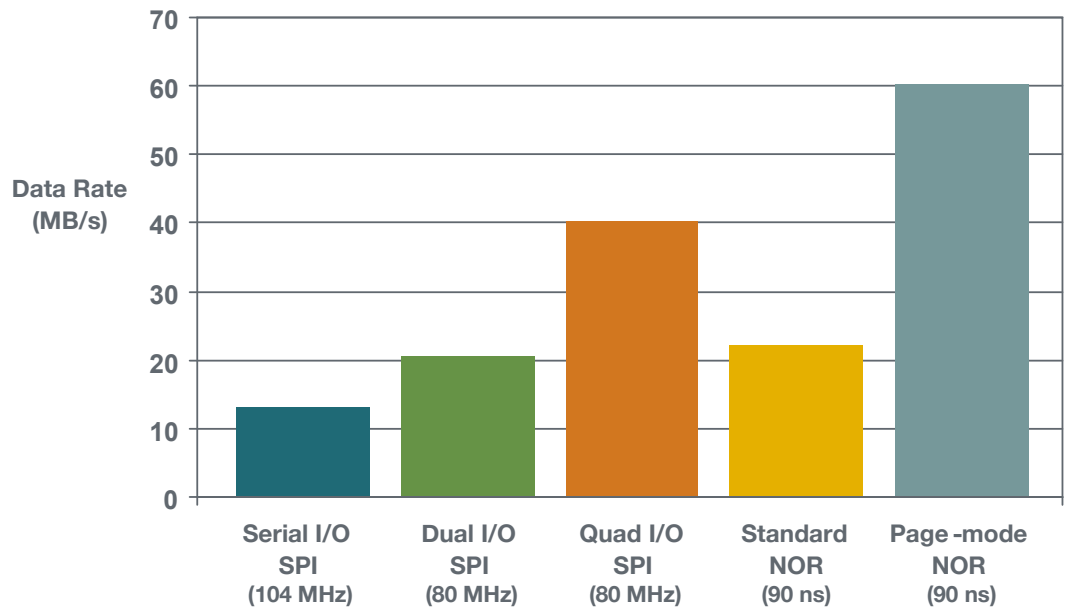
Today, SPI Flash memories must support increasingly higher performance with clock rates up to 80 Megahertz (MHz) in single bit mode. When an SPI Multi I/O device is used in quad mode operation, 80 MHz equates to running the flash at an effective clock frequency of 320 MHz with up to 40MB/s continuous transfer rate. This is more than six times the transfer rate of standard serial Flash memories running at a clock rate of 50 MHz. In addition to the fast data transfer, it also minimizes random access overhead by more than 70 percent compared to single bit mode by reducing the number of clocks required per read instruction (from 40 to 12). Table 1 shows a theoretical comparison between SPI and parallel NOR Flash memory interface. It can be noted that the dual I/O SPI is comparable to parallel NOR Word Read Mode while quad I/O SPI is about twice as fast.

Efficient random access is essential for eXecute-in-Place (XiP) operation. Assuming a typical instruction fetch of 32 bytes, the quad I/O SPI Flash memory is capable of random access rates of up to 40MB/s as depicted in figure 2. This outperforms 16-bit asynchronous parallel Flash memories (70ns access, 100ns cycle time) by more than 50 percent.

Application and system code continues to expand in end products which drives the need for higher density serial Flash memory solutions. To cope with the expanded data, it becomes essential to utilize quad I/O mode in order to achieve a faster boot up time, compared to single I/O SPI. For example, reading 32Mb of code would require about 670 ms at a typical clock speed of 50MHz (in single I/O mode). The same 32Mb of code can be read in about 105ms using Quad I/O mode at 80MHz (at an effective data throughput of 40MB/s). Similarly, utilizing 128Mb of code would require about 2.7 sec boot time in single I/O mode (at 50MHz clock speed), compared to only 0.4 sec in Quad I/O mode (at 80MHz). Hence, a 128Mb SPI flash device running at 80MHz in Quad I/O mode will boot almost 40% faster than a 4x smaller density 32Mb SPI flash device running at 50MHz in single I/O mode. Thus, as code size increases, higher densities would greatly benefit by switching to Multi I/O SPI mode.

In addition to its performance (in quad I/O mode) which enables faster XiP applications, Spansion MIO SPI Flash memory, also offers other important features commonly found in parallel NOR products—uniform erasable sectors for efficient memory allocation; storage of data; and security with lock-down and one-time-programmable (OTP) write protection.

FIGURE 2: DATA RATE COMPARISON OF SERIAL AND PARALLEL INTERFACES



CONCLUSION

By offering several benefits over parallel Flash memories, serial Flash memory is an attractive solution for a variety of applications. Lower system cost due to controller pin-count reduction, smaller and simpler PCBs, switching noise reduction, and lower power consumption in addition to high performance translate into a product primed for market acceptance.

Data referenced in this Spansion backgrounder is based on industry data, publicly available datasheet specifications, and feedback received through customers and chipset partner engagements.

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