Overview of Flash Based Embedded System Design

User Guide
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Chapter 1

Introduction

This User's Guide is intended for the exclusive use of Spansion® flash memory customers; the purpose of which is to call to the user's attention to operations and procedures outside of the control of Spansion, the original device manufacturer, that can have deleterious effects on the performance and/or later analysis of the flash device. In Chapter 1, the fundamental cell design of non-volatile floating gate flash memory is reviewed. Spansion also manufactures the patented MirrorBit® technology which is a 2-bit per cell variant to the floating gate flash but based on similar cell structure. The reader who is well versed in flash cell design and the basics of non-volatile memory data retention may want to move directly to Chapter 2 where we discuss some of the recommended best system practices with respect to hardware, software, and verification. In Chapter 3 the basics of PCB design layout is addressed in the interest of preserving good signal and power integrity for optimal performance. X-ray inspection techniques are addressed in Chapter 4 including set-up, peak energy, and dose recommendations to prevent adverse affects on programmed data. In Chapter 5, assembly and shipping considerations are discussed. Attention is called to storage of flash devices, effects of moisture and electrostatic discharge, and surface mount process recommendations to name a few categories. We conclude this document with Chapter 6 and a recommended board assembly and test manufacturing flow. By illustrating key system-level interdependencies we hope to enable our customers and system designers to avoid situations that either cause inadvertent violation of data sheet specifications or unnecessarily drive the flash memory to its lifetime limits. Our objective is to deliver the most robust, reliable flash memory to our customers for seamless integration into the vast number of applications in which Spansion NOR flash are used.

1.1 NOR Flash Overview

Flash is a generic term used for reprogrammable non-volatile semiconductor memory, a subset of the available semiconductor memory which has the capability to remove and replace data numerous times and which retains programmed data when there is no power to the device. Flash is available in a variety of embedded packaged forms which are soldered to boards as well as portable or removable forms, often with integrated bridge controllers to support common interface standards such as USB, SD or eMMC.

The two most popular embedded flash memory types are NOR flash and NAND flash. NOR flash is a type of non-volatile memory architecture to support fast random reads of individual bytes or words of data and high data integrity, ideally suited for applications such as embedded system controller boot loaders and PC BIOS. NAND flash is a type of non-volatile memory architecture to support high write speeds with read access limited to relatively large page transfers, ideally suited for applications such as memory cards in digital cameras. This document will discuss how to successfully implement designs utilizing Spansion's NOR flash products.

NOR flash is based on an architecture that allows for random accesses of individual bytes or words, similar to the SRAM. This random access capability enables processors to directly execute from code stored in flash, allowing processors to efficiently retrieve code or instructions located in random locations in the flash as the system software requires.

Individual NOR flash cells consist of a single transistor with source, drain and gate contacts. Sandwiched between the control gate and the channel (region between source and drain) is an electrically isolated storage medium. Charge can be injected or expelled from this storage medium (in a “flash”) and this charge
packet will not dissipate when power is removed from the transistor's contacts (meaning the cell is “non-volatile”). Programming a NOR cell involves injecting a packet of electrons into this storage medium by applying a high voltage between the control gate and the source when the transistor is operating with a specific source-drain voltage (see Figure 1-1). When reading, the presence of electrons in the storage gate alters the current flow through the channel region when a voltage is applied between the source and drain which is converted to a digital value, e.g. no current translates to a logic 0 and a measured current translates to a logic 1. The voltage across the source and drain where current “turns on” is commonly called the threshold voltage, $V_T$. Erasing of a NOR cell is the reverse operation where an oppositely biased high voltage between the control gate and the source moves electrons out of the storage medium creating a logic 1 state. Multiple cells are read in parallel to form a byte or words. Programming of cells occurs in parallel. And erase is performed in blocks of cells, also known as sectors. Multiple sectors are erased in parallel for uniformity and speed.

**Figure 1-1.** Floating Gate NOR Program and Erase

Spansion product family also includes a proprietary, patented charge trapping technology called MirrorBit. The MirrorBit cell functions on the same basic principles as the floating gate cell but doubles the density of the flash memory array by storing two physically distinct quantities of charge on opposite sides of a memory cell - a feat made possible by the non-conducting nature of the storage medium (see Figure 1-2). In this two-bit cell, each bit serves as a binary unit of data (either 1 or 0) that is mapped directly to the memory array. Reading or writing a bit on one side of a memory cell occurs independently of the data that is stored on the opposite side of the cell.

**Figure 1-2.** Floating Gate Compared to MirrorBit Cell Structure

A NOR flash device is driven by a host microcontroller, DSP or FPGA. For specific operations to occur, the NOR flash must successfully decode input signaling provided by the Host. For data integrity purposes, all operations that alter the data stored in flash require the Host to provide multi-cycle sequences of specific inputs. These command decoder input requirements are defined in individual device data sheets, which
include both command tables and descriptions of the specific requirements for enabling all supported functions.

Spansion offers several NOR bus/memory interface options, including:

- Address-Data-Parallel (ADP) - separate address and data buses
- Address-Data-Multiplexed (ADM) - partially shared buses
- Address-Address-Data Multiplexed (AADM) - fully shared buses
- Single-I/O Channel Serial Peripheral Interface (SIO SPI)
- Multi-I/O Channel Serial Peripheral Interface (MIO SPI)

Devices with either separate or shared parallel buses generally provide highest data rate performance due to parallel transfers of control signaling to the flash and parallel transfers of data from the flash. On the other hand, devices with serial interfaces provide reduced interface pin count enabling lower cost interface implementation. These five interface variations are industry standards which are supported by multiple NOR flash memory vendors as well as a large array of ASICs, micro controllers, DSPs, FPGA, etc... The selection of the appropriate physical interface option for an application depends on Host interface capabilities, system application and performance requirements, cost and other factors. The physical interface of a specific NOR flash is defined in its data sheet.

![Figure 1-3. Examples of NOR Flash Physical Interfaces](image)

1.2 Reliability

As part of Spansion's commitment to superior reliability, Spansion imposes a stringent set of reliability requirements on each of the products that we produce. Because of the vast array of products that Spansion sells, test requirements may vary based on the application, but strict attention is always paid to ensure the reliability of Spansion's products. Some definitions may be helpful in better understanding the variety of tests performed at Spansion:

**Reliability test:** A stress test performed on a representative, random sample of product designed to evaluate the reliability of a product or to help estimate its useful life.

**Life test:** A reliability test specifically designed for estimating the useful life of a product under normal operating conditions. It is usually an operating electrical test performed at elevated temperatures to provide thermal acceleration. Other types of accelerated stress are often applied -- voltage, power cycling, etc.

**Early life test:** An early life test is one specifically designed to evaluate that portion of the useful life of a product where parts with manufacturing defects would fail. It is of duration roughly equivalent to the first 4,000 hours of field operation and performed on a relatively large sample of the product in order to detect small percentages of defective product.
Inherent life test: A life test designed to evaluate that portion of the useful life of a product beyond early life portion.

In general, Spansion will establish a qualification plan based on historical data, experience, and critical elements (e.g. package design, customer requirements) which are aligned with and meet or exceed industry standards such as JEDEC, JEITA, IEC, and the Automotive Electronics Council (AEC). Additional information on reliability testing can be obtained by referencing applicable industry documents or Application Notes/Reliability documents applicable to the part number in question.

Two critical categories of non-volatile memory reliability important to any user's application are endurance and data retention. Endurance is a term used to refer to the number of times a flash memory cell, block, or sector can be erased and programmed in a reasonable amount of time without loss of device functionality. Data retention refers to the non-volatile cells ability to retain the charge packet stored within the transistor storage medium. As with all memory technologies there are practical limitations to lifetime and proper management of intended system operations (like program and erase) as well as inadvertent system effects (like thermal or electrical noise excursions) can greatly enhance NOR flash memory performance over time.

1.2.1 Program/Erase Endurance

To guard band system lifetime calculations, there are end-of-life parameters provided for Spansion flash customers that should be considered during system design as they place bounds on the usable life of a flash device. Data sheets provide the guidance on these end-of-life parameters. It is the objective in this section to explain why there are endurance limitations and explain the interaction of these end-of-life parameters so a system designer can properly assess the long term capability of their memory subsystem.

All erase operations in NOR flash are performed on one sector at a time, e.g. a chip erase operation is an internally managed sequence of individual sector erase operations. The high electric fields generated in the NOR cell during the erase operation create permanent physical defect sites as well as an accumulation of holes in the cell's bottom oxide layer separating the storage media and channel. A sufficiently high concentration of these aging related anomalies will result in the inability of a cell to either erase, program or read properly. It is important to note that all erase related cell degradation is contained within individual sectors. In other words, erase cycle accumulation in one sector does not contribute to the degradation of cells in any other sector.

Many flash families are guaranteed to support a minimum of 10k erase cycles per sector (a.k.a. erase block) under worst case usage conditions; however, typically NOR flash devices will support upwards of 100k or more erase cycles per sector prior to experiencing a significant percentage of failure. The probability of an endurance related failures varies by usage conditions, application stresses and most importantly the accumulation of sector erase operations.

The majority of oxide layer resident holes (a loss of an electron or a vacancy in the molecular structure) generated during an erase operation will dissipate naturally given adequate time between high electric field exposures. Data indicates that endurance related aging will be minimized when individual sectors accumulate less than approximately 1000 erase cycles per day. For this reason it is important to assess and constrain the erase cycle accumulation rate on individual sectors during long term system operation but also during manufacturing test and system qualification. Applications which perform rapid data logging should be constructed such that data capture is spread over enough sectors to assure no sector is erased more than ~40 times per hour. Applications which capture user data at power up/down events should not use fixed addressing as this can lead to high erase cycling even though the data capture volume is low.

Cell degradation as a function of erase cycling results in a gradual lengthening of the time required to complete an erase or program operation. Sectors with relatively infrequent updates will not experience significant lengthening of erase or program operations. Individual sectors which are frequently updated can be expected to experience up to 400% increase in sector erase times and up to 200% increase in programming times over the life of the device. Erase duration versus the number of erase cycles on a sector follows a curve similar to Figure 1-4. Not only is it importance to constrain erase cycle accumulation rates on individual sectors but also to employ watchdog timers to monitor these flash performance parameters in order to properly guard band total system performance. Data sheets and CFI (common flash interface) registers within the flash provide guidance on the maximum erase and program durations for proper watchdog definition.
1.2.2 Data Retention

Long term data retention requires the flash to tightly control the charge packet size in each cell during erase and subsequent programming operations. Transient variations in power and ground from spikes and noise during these operations can cause undetected variations in charge packet sizing that can reduce the long term ability to properly read a bit's programmed state. It is imperative that all noise and spikes on Vcc and ground be minimized via adequate filtering and layout. The reader may find more detail about system noise and suggested mitigation tactics in Chapter 4.

Long term data retention can be degraded by external factors such as excessive operating and storage temperatures as well as exposure to ionizing radiation such as naturally occurring cosmic particles and inspection techniques using X-ray to name two examples. The cosmic particles such as thermal neutrons result in charge loss due to atomic-level impact that induces short-lived charged particles and conduction paths. X-ray, an electromagnetic wave, can transfer enough energy to the stored electrons within the flash gate to accelerate the otherwise naturally occurring stored charge leakage. Higher temperature thermal environments can have a similar effect. These external factors degrade the long term ability to accurately read a programmed bits, e.g. 0 bits. Thermal storage and operating limits are listed in each product data sheet. X-ray inspection guidelines and suggested manufacturing assembly and programming sequencing are reviewed in Chapters 5 and 2, respectively.

Long term data retention is also affected by the erase cycle induced cell aging effects discussed previously. For example, data retention for all commercial MirrorBit is specified as 10 years guaranteed and 20 years typical when operated or stored within the data sheet specified operating temperature range. This specification applies to relatively lightly exercised sectors, e.g. those with <100 sector erase cycles. Users should expect sectors that are more heavily cycled to have correspondingly less data retention capability. The implication of this interrelationship is that sectors used for shorter term data storage which are heavily cycled have inherently less data retention capability. This generally does not create a system level problem because frequently replaced data implies a lower data retention requirement for that data set which in turn the flash can readily support. The following is an example to illustrate to the user how to assess inter-related endurance and data retention system requirements.

Example: A system has a required 10 year life cycle and certain sectors used for event logging can be expected to accumulated 10k erase cycles. This equates to 1000 erase cycles per year with an average data retention requirement of ~ 1/3 year. If the data retention for the flash can be expected to be 2 years after accumulating 10k erase cycles, there is a 500% margin in flash effective data retention capability to system requirement.

Characterization has shown that the relationship between data retention capability and erase cycling, a.k.a. endurance, varies as a function of operating temperature. Specifically, lowering the operating temperature from 85°C to 55°C has shown to increase data retention as much as 1000%. Data sheet specifications are provided for worst case conditions, e.g. 85°C.

For more detail on the interaction of endurance and data retention, please refer to Spansion application note: http://www.spansion.com/Support/TechnicalDocuments/Pages/ApplicationNotes.aspx.
Significant advances in the science of NOR flash memory design and manufacture since its introduction in the early 1990s have resulted in well controlled and reliable mass production of NOR flash. Internal circuits exist to compensate for real world variations in temperature and electrical environment such as noise and fluctuations in power, glitches and spikes on input and outputs, etc. Spansion data sheets define how the flash will reliably perform under strictly defined usage conditions. This User Guide contains a variety of additional insight into how to take some precautions in system design and operation, to manage your true cycling requirements, in order to manage flash data storage for optimal performance as well as mitigate some environmental variations that are undesirable over the life of an electronics system.
Chapter 2

Recommended Best Practices

2.1 Basic System Hardware Considerations

The following discussion addresses a number of basic hardware related details with respect to the Host controller to flash interface, operational configuration, flash bias supply, and the flash/module operating environment. The information being addressed is fundamental and should be considered when designing an embedded system utilizing NOR flash memory.

2.1.1 Host Controller to Flash Interface and Operational Configuration

The selected embedded controller or “Host” most often defines the type of flash which will be selected and the specific bus configuration. There are basic systems level choices whether to use a parallel NOR (asynchronous, page, or synchronous accesses) or SPI flash (single or multi I/O) as previously defined. The Host to memory interface is typically straightforward but a designer using parallel NOR must be aware of whether the Host address bus supports byte (x8), word (x16) or double word access (x32). For example, Spansion S29GL256P can be configured to support word or byte accesses, but in either case address line A0 controls word address and needs to be interfaced appropriately to the system address bus. Please reference Spansion’s Application Note Connecting Spansion Flash Memory to System Address Bus for additional details: http://www.spansion.com/Support/TechnicalDocuments/Pages/ApplicationNotes.aspx.

The flash operating mode is defined in some cases by a simple pull-up or pull-down tied to a flash input signal. For example in the S29GL256P, the “Byte#” signal input logic state defines whether the flash read and write accesses are in byte or word mode. On the other hand the Spansion S25FL129P supports a configuration register which is setup with default states at power-on. Utilizing the configuration registers, this Spansion product can remain in default single I/O read/write mode or can be reconfigured to support multi I/O read/write accesses, depending upon the user’s system requirements. Please reference the product data sheet of interest for additional details regarding configuration options and appropriate means to modify configuration setups.

2.1.2 Flash Bias Supply and Operating Environment

Providing the flash an appropriate operating environment is essential and basic to reliable flash start-up and operation. Prior to entering discussion of these topics; the following information is provided as a base line to understand two essential items covered in the flash data sheet which are Absolute and Recommended Operating Conditions.

The absolute maximum operating conditions define the electrical and thermal parameters which are never to be exceeded. Exceeding these defined conditions can damage the flash silicon which would compromise the reliability of the device’s current or future functional operability. Appropriate oversight and planning should be utilized to assure that the flash Absolute Maximum Operating conditions are never exceeded.

The data sheet also provides the recommend operating conditions for the flash device. Prior to delivery the flash is fully tested and verified to meet the data sheet specifications. Operating the flash device outside the conditions specified in the data sheet could result in access failures including but not limited to read failures or failure to start or properly complete an embedded operation. It is recommended to verify that a system
provides the flash device an operating environment which at a minimum meets the data sheet recommended operating conditions.

### 2.1.2.1 \( V_{CC} \) Power On / Power Off

Appropriately applying \( V_{CC} \) bias to the flash is the first step to complete prior to accessing the flash device. The flash data sheet lists the Vcc power on and power down requirements. These are typically provided in terms of voltage bias level, required ramp characteristics, and power on reset timing (POR). It should be noted that if system start-up does not comply with the data sheet recommended start-up conditions, it will result in device inoperability. Note the reason for these start-up constraints is that NOR flash has several key functional areas such as the embedded algorithm controller, pre-amplifiers, cells array, and other areas which must be appropriately biased prior to use. A flash embedded controller requires a finite define period of time after valid \( V_{CC} \) has been applied to complete its initialization process before it can respond to the system or Host controller. Best practice is to ramp \( V_{CC} \) and \( V_{CCQ} \) together at a continuous ramp rate of approximately 10 µs/1V, without RST# and CE# toggled.

![Figure 2-1. \( V_{CC} \) Power On Ramp](image)

It is assumed in the flash data sheet specifications that the device is operating under continuous power. In embedded applications, continuous power is not always reasonable or practical. If a power interrupt occurs during an embedded program or erase operation, the flash array data cannot be trusted. In Section 2.2, software methods for power interruption recovery are discussed. But from a hardware perspective, if software does not check for erase operation completion, the erase command should be re-issued upon power restoration. In addition, if the system software is configured to sense an impending power loss, flash operation can be suspended before \( V_{CC} \) drops below the minimum operating range. Power loss can be delayed by capacitors or point-of-use power supplies long enough such that the flash can complete its embedded operations or be suspended safely. If there are no assurances that the erase sequence has been completed or terminated before \( V_{CC} \) drops below the data sheet minimum operating limit, an erase command should be re-issued after power is restored.

### 2.1.2.2 Power Supply Considerations

An important topic related to the flash \( V_{CC} \) bias is the module's power distribution network and signal integrity which can directly affect the flash operating environment in terms of bias noise levels and ground bounce. The flash \( V_{CC} \) noise levels can directly affect the reliability of flash read, program, and erase operations.

A flash device has both analog and digital sections. During a flash read operation, Row and Column Decoding are used to select subject cells in the flash array. The subject cell's IDS current will be an \( I_{\text{Erase}} \) or \( I_{\text{Program}} \) based on the charge stored in the cell. The subject IDS current is output to sense amplifiers where it is converted from an analog signal to a digital signal and captured in the output buffers. The major flash blocks used to complete this read process are depicted in Figure 2-2 below:
Critical internal flash analog signals and reference voltage(s) in the pre-amplifier, charge pumps and cell array sections should operate in an environment which allows maximum read margins, stable internal references and reliable operation. If this is not the case and the module level $V_{CC}$ noise and ground bounce increase, the previously cited read margins will decrease resulting in less reliable read operation. Under extreme noise conditions the read margins can collapse resulting in read failure. These same principles apply to flash program and erase operations where these same read margins and internal references can be compromised as the $V_{CC}$ noise increases.

Figure 2-3 shows two examples of $V_{CC}$ supplying flash ICs. The $V_{CC}$ on the left is a case where noise has been mitigated and the voltage is stable and within the upper and lower limits over time. The $V_{CC}$ on the right exhibits significant voltage fluctuation verses time and there are excursions where the voltage level is outside the desired limits.

A well designed power delivery network (PDN) is essential to mitigate $V_{CC}$ and ground plane fluctuations; $V_{CC}$/ground noise is typically the result of circuits switching inside the semiconductor devices and at the device interface. Faster signal slew rates with newer, higher performing devices increases this challenge. Noise from the signal transitions are coupled to $V_{CC}$ and ground by parasitic impedances. Inductance is a critical parameter in noise generation during signal switching and is primarily introduced by package and PCB physical features. The electrical performance of a power and ground system is typically characterized by its impedance across the switching current frequency spectrum.
In *Chapter 3* we will revisit power and signal integrity and address some basics with respect to PCB design and good PDNs. Other hardware considerations during system design that can compromise the quality of the power delivery include the use of long transmission line lengths between the Host controller and the flash memory, decoupling capacitance positional placement and values, added parasitics from connectors or daughter cards placed between the controller and flash, etc. System designers should characterize and optimize module level signal and power integrity to ensure flash recommended operating conditions specified in the data sheet are met.

For further reference for system designers:


### 2.1.2.3 Thermal Operating Conditions

Spansion flash devices are functionally tested at the maximum operating temperature. This testing at maximum operating temperature greatly simplifies the flash thermal consideration allowing Spansion to stand behind the flash data sheet specification for operation in a thermal environment up to the maximum operating temperature. In any system design it is recommended to characterize the flash thermal operating environment through measurement and simulation. This process typically includes characterizing the module's air temperature and velocity and PCB temperature close to the flash unit. In some cases it may be required to measure the top of the flash unit for more accurate simulation purposes. Spansion NOR flash is a low power device and most often in the system environment, thermal concerns are related to other higher power devices heating the lower power NOR memory. To more accurately predict the thermal performance of the system and components therein, the user may apply finite element models (FEM) and computational fluid dynamics for comprehensive simulations. Spansion as a component supplier can act as consultants or actively assist in thermal simulations. Please contact your local representative for further information regarding system level simulation.

### 2.1.3 Flash Accesses Timing

The flash AC operating characteristics define the required timings to access a flash device to perform read, erase, or program operation. The flash data sheet provides very detailed timing specifications and diagrams showing the setup and hold conditions for control signals, address and data lines for each type of flash access. It is critical to thoroughly review the controller timing specification to ensure its minimum and maximum setup and hold times have been configured to meet the minimum and maximum timing requirements for all utilized flash accesses across all operating conditions.
2.2 Basic System Software Considerations

There are several different interfaces used to write data to flash. At some level, a flash driver is needed to manage the data in the flash array. A common approach includes an application that calls operating system services to store data in files on a disk. The file system writes disk sectors to a flash block driver, which allows a flash device to appear like a hard disk. Disk sectors are the minimum granularity for any write from the file system to the disk. The most common disk sector size is 512B. In order to update one byte of a file, the file system would overwrite the appropriate disk sector. The block driver calls a flash abstraction layer that contains commands specific to a flash device or type of flash memory. The flash abstraction layer sends commands to the flash device through firmware or a flash controller. Different systems may have various combinations of these software layers.

![Figure 2-4. System Software Stack](image)

Regardless of the application or file system interface, and the complexity of the driver, data needs to be stored in the flash device by programming. Most applications need the ability to store and update data with a finer granularity than the flash device can erase (typically 64 kB or larger). The data can be written in smaller increments, but an update is more complex with flash than it is with RAM or a hard disk. Because of the large erase size, it is more efficient to program the new data to a different location, and use some mapping system between the address from the application or file system, and the flash address. This indirect method requires the flash driver to maintain a pointer to the most up-to-date data for a given virtual address. For embedded systems, the mapping information is stored in flash, so that it persists when power is turned off. This extra data is called metadata to distinguish it from data written by the upper levels of software.
2.2.1 Partition and Format

NOR flash memory is often used to store both code and data. Software will generally divide the memory into partitions. One partition could store code that is rarely updated using a direct or raw format, so that the code can be executed directly from the flash. Another partition could store data like a virtual hard disk.

**Flash Partition Example**

<table>
<thead>
<tr>
<th>code partition</th>
<th>data partition (flash disk)</th>
</tr>
</thead>
</table>

Format is the term used to describe the organization of data and metadata on a disk (or other media). Software that manages a flash device will impose some format on flash to manage the data. Typically, file data and metadata are written at the same time. These writes may be a single flash program operation, or they may be two separate program operations in distinct areas of memory.

**Flash Disk Format Example 1**

- “d1” represents data element 1.
- “m1” represents metadata for “d1”.
- “d2” represents data element 2.
- “m2” represents metadata for “d2”.

**Flash Disk Format Example 2**

<table>
<thead>
<tr>
<th>data entries</th>
<th>metadata entries</th>
</tr>
</thead>
<tbody>
<tr>
<td>d1</td>
<td>m1</td>
</tr>
<tr>
<td>d2</td>
<td>m2</td>
</tr>
<tr>
<td>d3</td>
<td>m3</td>
</tr>
</tbody>
</table>

Although flash memory can only be programmed from 1 to 0, metadata entries may be updated several times to record state transitions. For example, when the file data is first written, the metadata might indicate a “valid” state. When the virtual disk sector is updated, the previous entry might be marked “invalid”. Eventually, most of the erase blocks (flash sectors) will contain both valid and invalid sector data. At some point, a block will be chosen for erase, and all valid entries will be moved to a fresh block.

<table>
<thead>
<tr>
<th>State (hex)</th>
<th>State (binary)</th>
<th>Flash Memory Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFh</td>
<td>11111111b</td>
<td>unused</td>
</tr>
<tr>
<td>7Fh</td>
<td>01111111b</td>
<td>valid entry</td>
</tr>
<tr>
<td>3Fh</td>
<td>00111111b</td>
<td>invalid entry</td>
</tr>
</tbody>
</table>

Before choosing a data format for the flash disk partition, consider the data sheet requirements for all the flash devices that might be used. When a single binary image file is programmed on the assembly line into multiple flash families, a single flash disk format must support all of the families. Some devices might have smaller erase sectors than others. Some devices might have boot sectors. There could be a subtle difference in the programming requirements. For devices to meet the specified endurance and to maintain data integrity in field operation, software must follow all the requirements of each specific device. Ignoring the data sheet requirements can lead to system failures that are difficult to diagnose.
2.2.2 Programming Data Reliably

Spansion flash reliability meets or exceeds market requirements when used according to data sheet specifications. However, extra precautions can be employed to handle unexpected situations, particularly for critical data.

Programming data to the flash is most efficient and reliable when writing in increments of the maximum size. For SPI flash, write full pages, once per page, aligned to a page boundary. For parallel NOR flash, write full write buffers, once per buffer, aligned to a buffer boundary.

For many applications, writes are needed at a smaller granularity. Consult the Spansion flash data sheet for the recommended program size, and the ramifications for multipass programming. Some devices allow bit-walking (multiple program operations that clear a single bit at time) within the specifications for data reliability and retention. On other Spansion flash devices, this operation may lead to degradation in the specified endurance and retention.

For example, the recommended minimum program size for MirrorBit NOR devices is a Program Block (16 bytes). If critical data is stored in multiple programming operations within a single Program Block, then a software validation method could be used to ensure the data retention and endurance of critical addresses. A cyclic redundancy check (CRC) could be used to detect errors. Another option is to employ an error-correcting code (ECC) to repair any single bit errors. And storing multiple copies is yet another option for safe-guarding critical data.

Many applications require flash software to provide atomic operations. In this case, when a file update is interrupted due to power loss for example, rather than losing the file completely, the file is rolled back to the previous version. This requires the flash software to preserve the previous file data until the updated file is completely written. Software may scan all file entries at startup, or it may check each file as it proceeds to use them. When and invalid file entry is detected, the driver can take action to recover the last known good version of the file. The Linux JFFS2 flash file system is an example of such an approach. In JFFS2 all nodes, i.e. data updates, are protected by an individual CRC. If this CRC is erroneous due to a power loss than the node or data update is ignored and the file system rolls the view back to the last consistent state.

2.2.3 Maximize Programming Throughput

To maximize the throughput from the processor to the Spansion flash device, it is important that the data being transferred is aligned to the size of the data bus. Programming data in full, aligned pages (or write buffers) is the fastest method to store data. Using misaligned buffers will force alignment at some level of software or firmware. This can slow down the system. Please consult the documentation for your processor to understand the impact on your platform.

Some flash families support unique commands that allows faster programming to the flash array. For example, several Spansion parallel NOR devices can use accelerated (high voltage) programming, and MIO SPI devices support Quad Page Program, which transfers four data bits in a single clock cycle, rather than the classic single bit for SPI devices.

Manufacturing environments can push commands, address, and data to multiple devices in parallel. Avoid bus contention by only allowing reads from a single device at a time. This includes status reads.
2.2.4 Wear-Leveling

Each flash device is rated for a certain number of erase cycles. After this amount of wear on the flash array, it is no longer expected to meet the specifications for performance and reliability. Wear-leveling is a method to distribute erase cycles evenly across the flash array to extend the effective lifetime of flash memory.

Flash memory areas used to store boot loaders, operating system images, or other executable code, are generally erased less frequently. These areas are considered static. Areas used to store data, like file system partitions, are generally erased more frequently. These areas are considered dynamic. Dynamic wear-leveling solutions will only distribute flash usage across the data partition, while static wear-leveling solutions manage both data and code partitions. Please consult your local field representative to determine if software wear-leveling (dynamic, static, or some combination of both) will be advantageous to your specific memory subsystem. Refer to the Wear Leveling application note (http://www.spansion.com/Support/TechnicalDocuments/Pages/ApplicationNotes.aspx)

2.2.5 Suspend and Resume

Erase operations can be suspended to program or read the flash. Program operations can be suspended for reading. On SO (simultaneous operation) products reading of one bank can occur while simultaneously writing to another back, but the Suspend and Resume commands can be used when accessing the same bank. It is possible to issue suspend and resume commands for an operation at such a high rate that the operation will not make any progress toward competition. So allow enough time between a resume and the next suspend for the operation to proceed. For example, a minimum time of $t_{ERS} = 100 \, \mu s$ is recommended between Erase Resume and another Suspend command on some SPI devices.

In addition some Spansion flash devices report the status of suspending an operation. Consult the data sheet for details. For example, on one such data sheet it is indicated that Status Register 2 contains Erase Suspend and Program Suspend bits to indicate whether these operations are suspended.

2.2.6 Erase

Flash devices are rated for tens or hundreds of thousands of erase cycles at any given location. However, erase cycles should not exceed 1000 per day. Some companies that incorporate Spansion flash devices into their designs will try to shorten qualification time lines by increasing the number of cycles per day. This is an acceptable approach, but exceeding the 1000 cycle per day limit could introduce artificial damage that leads to a failure mechanism that does not represent true field failures.

If power loss interrupts an erase operation, the command must be issued again after the system power has been restored. When power loss is expected to interrupt erase operations, software must be designed to detect partially erased blocks. Since the contents of such a block are indeterminate, a signature or some state information can be used to verify each block. Software may scan all blocks when power is restored or it may check each block as it proceeds to use them. In Linux for example, the JFFS2 flash file system writes an erase block marker (a special 12 byte pattern) at the beginning of a sector after it has been successfully erased. If this marker is missing the sector has probably seen a power interrupt and will be rescheduled for another erase operation.
2.2.7 Polling Status

After issuing an erase or program command sequence, software can read from the flash to check for completion of the operation. Polling is the process of reading the status periodically until the device indicates the operation is complete. Check the data sheet for a particular Spansion flash device to determine the available methods to check status. The following are some of the possible methods:

- Data Polling
- Status Register
- RY/BY# pin

When software uses Data Polling to check the status of an embedded flash operation, the error bits should be checked while the device is busy. If an error is detected, the status should be read again to determine if the transition from busy to complete created a false failure status. When software reads from a Status Register, error bits should be checked once the device is ready. Some SPI (Serial Peripheral Interface) have error bits in the Status Register and others do not. Check the data sheet for specific details on any particular device. When handling an error detected, software should clear any Status Register error bits. Clearing error status is unnecessary with Data Polling.

Polling reads for program status should be separated by at least 100 µs and at least 100 ms for erase status reads. More frequent polling or status reads could generate noise on the power delivery network as both operations involve I/O switching and the respective current transients.

Software should poll the flash device status for completion after initiating the following operations:

- Sector Erase
- Chip or Bulk Erase
- Word, Write Buffer, or Page Program
- Write Registers
- PPB Erase
- PPB Program
- Write PPB Lock Register
- Password Program
- Password Unlock
- Wear-Leveling Disable Bit Program

2.3 Verifying Basic Flash Operability

Flash basic operability can be defined by three fundamental operations read, erase and program. For the purpose of these discussions it is assumed that the system design under consideration has proven basic functionality and the intent is to determine if a system level issue can be isolated to a flash related fault in term of read, erase, or program. A high level overview of the flash operational modes is captured below:

The Read operation enables access to digital data contents of the flash memory array. To reiterate, Spansion flash products support parallel or SPI read modes. A parallel flash may support standard asynchronous, page, and/or synchronous read accesses; while a SPI flash may support Single and/or Multi I/O read accesses in standard, fast, or high performance mode.

The Programming operation sets a bit or group of bits from 1 (erased) to 0 (programmed) and can be performed on a bit, byte word, or page basis. During internal device programming, program pulses are directed to subject cells to be programmed followed by verification of the subject cell’s charge level using internal references to determine if the subject cell is appropriately charged. In the case when the cell is not sufficiently charged the process of program pulse followed by verification is repeated.

The Erase operations converts bits from 0 (programmed) to 1 (erased) and are performed on a sector basis. The erase operation first precondition the sector and then launches internal operations which complete erasure of a subject sector(s) with maximum reliability. The preconditioning or preprogramming operation internally programs (or verify) all bits in the sector are to a “0” state. The pure Erase operation erases all bits in the array in parallel followed by Post Erase Conditioning which optimizes Erase charge state.
2.3.1 Read Verification

Performing read verification is the initial step to be completed for all suspected flash failures. First, perform a basic read of the Flash Mfg ID and Device ID. This will determine if the system controller is communicating with the flash device correctly and provide good indication of basic continuity, appropriate access timing, and voltage bias. If the flash device fails in the original system, it is highly recommended to re-verify these basic Read operations on a reference system such as an industry standard flash programmer and determine if the reference system successfully completes the read verification steps. If the read verification fails on both systems then the flash should be examined for signs of mechanical stress or electrical overstress. Work with Spansion technical support team to validate the observed failure.

If the first step passes, the second step is to determine if the flash array has good stability and integrity under the module operating conditions. This can be completed via capturing and recording any addresses where read failures occur in the flash array.

Example: Master Pattern verses Flash Dump

Always try to capture the "actual" failure analysis (FA) data set for the read failure verses relying on high level information like there was a checksum failure:

- Confirm and document file comparison between the original master pattern and current flash dump: (Any flash areas which have been erased and reprogrammed with new data will have mismatch errors against the master pattern)
  - Example:
    - Document observed read mismatches as follows
    - address(es) of all confirmed read failures
    - expected and actual data at these locations
    - Capture flash read mode used during observed read failure.

2.3.2 Program and Erasure Verification

After completing the read verification and the device is shown to have good read integrity one can proceed with Program verification followed by Erasure verification. It is essential to understand the system programming and erasure algorithms, any block protection, and time out constraints (for example a system auto-timer used rather than status polling). Monitoring the embedded operation status bits or status register during Program or Erasure is the recommended means to determine if the embedded operation was completed successfully. Note, the device data sheet defines each status bit in detail. Both Programming and Erasure operations should be verified across the specified flash VCC operating range.

The following are a couple of examples looking at S25FL129P's status bits:

1. During programming the WIP and P_ERR indicate if the Program Operation completed successfully or if there was an error. In instances where P_ERR = 1 (Program Error) is observed during a program operation a device fault has occurred.

2. During Erasure the S25FL129P status bits WIP and E_ERR indicate if the Erase operation completed successfully or if there was an error. In instances where E_ERR = 1 (Erase Error) is observed during an Erase operation a device fault has occurred.

Additionally, by reading the Status Register WIP bit after sending a program or erasure command the user can conveniently see whether the device successfully accepted the command to initiate the embedded operation.
2.4 Summary

As we have discussed, there are some design and operational considerations that must be taken into account to address the interdependencies within the system level memory to controller interface and to utilize the flash memory with the greatest efficacy. The configuration, electrical budgets, timing, data format, etc. of the flash and the Host controller must be aligned. The operating environment, both electrical and thermal, can affect various operating budgets. All these consideration can affect the flash performance which in turn affects the system performance and reliability. In this section we have called out categories with regard to recommended system best practices which include hardware and software considerations as well as procedural steps to verify the memory subsystem is operating as expected. This short section is not entirely comprehensive but your local Spansion field representative can expand upon any or all of the topics and guide you with respect to your specific Spansion flash product.
Chapter 3

PCB Layout Guidelines for Signal Integrity

3.1 Introduction

Signal integrity (SI) describes how well a signal maintains its desired shape and how the signal characteristics affect the receiving device's ability to perform the desired operation. A signal loses fidelity/integrity when it becomes distorted or when the signal-to-noise ratio (S/N) degrades. Two of the aspects associated with SI are signal reflections due to source and load impedance mismatches and noise generation associated with signal switching and parasitic impedances. With today's high-speed digital designs, fast slew rates and parasitic impedances can result in additional signal and $V_{CC}$ noise resulting in reduced read margins and operational reliability. Every design is different but in many cases SI problems begin showing up when slew rates approach the nanosecond range or faster. Fast switching signals and associated trace inductance contribute to noise generation. All signal traces have inductance and the voltage generated across an inductor can be approximated by $V_l = L \frac{di}{dt}$, where $L$ is the trace inductance and $\frac{di}{dt}$ is the rate at which the current is changing. The voltage $V_l$ across an inductance increases proportionally with the rate at which the current changes. $V_l$ across the trace inductance combines with the original signal and is seen as noise. The more switching current that occurs simultaneously or in rapid succession, the larger the electrical noise becomes and can be seen as variation, or ripple, on the system power supply. This noise couples to the signal of interest and if severe enough can cause the signal to be detected incorrectly (on instead of off, high instead of low, etc.).

In the example below (Figure 3-1) signal overshoots and undershoots can be seen. Channel 1 shows the $V_{CC}$ bias before and after noise is introduced. A control signal on channel 2 displays the effects of the noise.
Power supply integrity and the importance of maintaining low noise levels on the power supply to the flash has been emphasized. Package selection and PCB design can play important roles in either worsening or mitigating power supply noise. Furthermore, signal fidelity must be preserved from transmit to receive between the flash device and the host controller and depends on the same physical design features as power integrity. In this chapter we will briefly discuss some good practices with regard to PCB design.

3.2 Power Supply

All ICs benefit from a low noise power supply. Fluctuations on power and ground nets can occur for a variety of reasons. One reason can be a change in load current drawn from the supply net due to simultaneous operations either between multiple devices on the net or by multiple operations within one device. For example, read and write, referred to as simultaneous operation (SO) within the flash device or simultaneous switching of outputs can cause variation in load current. The noise generated on the power supply network can range in frequency from a few kHz to GHz. Firstly, power and ground planes should be placed such that there is uniform, uninterrupted coupling between the current path into the device and its return path. In addition these solid (or nearly solid as vias are inevitable) planes provide a solid reference for signal nets. Signals should be routed over their reference plane and not bridging over one plane to the next in a split plane configuration. Secondly, proper use and placement of decoupling capacitors are recommended. When noise frequency is low a larger bulk capacitor (for example, 4.7 µF) between the power and ground planes removes this noise. Smaller capacitors (for example 2.2 µF, 0.1 µF, and 0.01 µF) placed near to and around the flash device can reduce higher frequency noise. Low ac impedance between the power and ground should be maintained. Local impedance spatial plots as a function of frequency can be modeled and simulated with a variety of commercially available signal integrity software tools. Spatial plots are a convenient way of viewing the impedance of the PCB in the vicinity of the memory and the controller ICs. These tools and techniques can aid in strategic decoupling capacitor value selection and placement.

The routing of the capacitor (normally 0603 or 0402 package) should be optimized to achieve lower inductance. It is recommended to keep the power trace length (from the package pads to the vias) shorter with the trace width around 24 mils. Also, it is good design practice to avoid sharing the same via with 2 or more decoupling capacitors. Figure 3-2 shows examples of routing the decoupling capacitor.
3.3 Clock Signal Routing

In high speed synchronous data transfer, good signal integrity in a PCB design is of importance, especially for the clock signal. When routing the clock signal, special cares should be taken. The following practices are recommended.

- Run the clock signal at least 3x of the trace width away from all other signal traces. This helps to reduce unwanted coupling to the clock signal. See Figure 3-3.
- Use as few via(s) as possible for the whole path of the clock signal. Vias will cause impedance changes and signal reflection.
- Run the clock trace as straight as possible and avoid using serpentine routing except for some specific cases where it is desirable to introduce additional clock line delay. See Figure 3-4.
- Keep a continuous ground or power plane in the next layer as a reference plane and avoid split plane designs where signal traces bridge over multiple planes.
- Route the clock trace with controlled impedance.
3.4 Data Signal Routing

In order to keep the correct timing for the data transfer, in the PCB routing, the data traces should match the time delay with the clock trace from the host controller to the flash. The data signals should be routed with traces of controlled impedance to reduce the signal reflection. Avoid routing traces with 90° angle corners. The recommendation is to cut the corner and smooth the trace when trace route needs to change direction. Figure 3-5 shows an example of trace routing at the corner. To further improve the signal integrity, avoid using multiple signal layers for data signal routing. All signal traces should have a continuous reference plane.

Figure 3-5. Signal Routing at the Corner

3.5 Layout Simulations and Validations

The previous sections highlight some recommendations and guidelines to assist designers in optimizing the local flash power supply and Signal layout. The goal of this information is to assist the designer's realization of a valid flash operating environment in terms of that both the flash $V_{CC}$ and I/O signals meet system specifications and are non-monotonic signals. Section 2.1.2.2 on page 12 details how the flash operating environment directly affects its internal references, read margins and overall functional reliability. Spansion recommends the use of this information during both the design simulation and validation phases.

Spansion provides multiple types of simulation models for Spansion flash memory devices which can be utilized during the design simulation phase. For signal integrity simulations Spansion recommends using IBIS (I/O Buffer Information Specification), which is a behavioral description of the I/O buffers and package characteristics of a subject semiconductor device. The IBIS model format was developed a consortium of semiconductor companies to provide customers the data required to perform more timely signal integrity, EMI, and transient simulations without needing proprietary based HSPICE models.

Many PCB design houses utilize pre-layout and post layout simulations phases to define high level constraints followed by optimization of critical areas once the initial full layout realized. The pre-layout simulations are employed at the earliest stages of the PCB design and are intended help define PCB design variables such as topologies, component placement, general board layout/stack-up; termination usage and other variables. During the pre-layout phase these items can be easily be manipulated to provide understanding of trade-offs associated with different configuration options. In addition, these simulation results help to set crucial parameters for the transmission structure, such as trace width, trace spacing, maximum trace length, and critical component placement thereby defining the layout rules. Once the initial layout is complete, post layout simulation can be performed, and incorporate required layout changes to mitigate observed signal integrity issues. The overall objective is to lay the foundation for acceptable signal characteristic and $V_{CC}$ performance. The Initial design is typically scrubbed via simulation and design review processes prior to and prototype fabrications.

The empirical validation phase can be initiated upon prototype fabrication. A key empirical validation process is Signal integrity (SI) testing which can be described as the process of capturing, evaluating and correcting any identified signal characteristics issues. Empirical SI evaluations can be very beneficial during the earlier prototype development stages. Signal characteristics are commonly captured via oscilloscope measurements; this process can be very time-consuming. It should be noted that measurement equipment and techniques used to capture the signal characteristics can have a significant effect on the signal integrity. The addition of parasitic impedances can be a real problem leading to the creations of an issue or real issues may not be observable as measurement tools are introduced. These types of issues will only become more difficult to address as bus frequency continue increasing.
3.6 A Check List of Recommendations

The following is a check list of PCB design recommendations.

- Place decoupling capacitors as close as possible to the flash device and in the current path to the device. A value of around 0.1 µF ceramic capacitor with 0603/0402 package is a good starting point.

- Clock should be routed straight and with minimum vias if possible. Separation of clock and other signals is important to keep the clock clean.

- All signal traces should have a solid reference plane (either GND or V\text{CC}) in an adjacent layer.

- All signals should be routed with controlled impedance. Typically, the PCB is recommended to be built of 50Ω trace impedance with ±5% tolerance.

- The data bus should be routed with matching length to the reference of the clock. The matching length is recommended to be within ±150 mils.
Chapter 4

Impact of X-Ray Inspection on Flash Memory

4.1 Introduction

X-ray inspection is a commonly employed method used to gauge the quality of solder connections on surface mounted BGA packaged devices on printed circuit boards. It has been well established that semiconductor ICs can suffer damage from (dis)charging effects caused by X-ray energy. This document is intended to help customers who perform X-ray inspection during their assembly process with guidance on the assessment and mitigation of risks associated with X-ray inspection of Spansion flash memory components.

4.2 X-Ray Inspection Impact on Programmed Data

X-rays behave basically the same as visible light rays, since both are wavelike forms of electromagnetic energy carried by photons. The difference between X-rays and visible light rays is a 10,000-fold difference in energy for individual photons, which is inversely proportional to wavelength. X-rays have been shown to perturb the threshold voltage (Vt) of individual programmed bits within flash memory arrays. A sufficiently negative change in the Vt of a programmed bit will result in the incorrect sensing of the programmed bit logic state during a read operation, e.g. a read data operation incorrectly returns a logic state of “1” when it should return a logic state of “0” for a programmed bit. The impact of a read failure on system performance can range from benign to catastrophic.

A variety of factors influence the programmed bit Vt change, including:

- **X-ray energy spectrum**
  X-ray radiation has been found to affect programmed Vt. Soft x-rays in the energy range of 2-9keV are absorbed by silicon and damaging to flash memory cells. Adequate X-ray inspection imaging does not require X-rays in the <9 KeV energy spectrum. Analysis has shown that 50 µm Cu traces are best imaged with X-ray energy of 9-20 KeV and that solder components, e.g. tin and lead, are well imaged by X-rays over the energy range of 10-50 KeV.

- **X-ray inspection equipment**
  The size of the changed Vt population (number of bits affected) has been found to be affected by dose, which varies as the square of the KVpeak used during inspection, linearly with tube current, and inversely with distance from X-ray tube to flash device being inspected. X-ray energy and flux (dose rate) vary significantly among commonly used X-ray inspection equipment. Laminography-based equipment, such as Agilent 5DX, has been found to be particularly damaging to flash memory due to its highly concentrated, uncollimated and powerful X-ray beams.

- **X-ray exposure time**
  The number of bits affected increases linearly with X-ray inspection time. However, programmed Vt change is NOT linear with dose or time. The change in programmed Vt varies as the square root of time, while dose varies as the 1.5 power of time.

- **Flash semiconductor process feature size**
  Flash semiconductor process feature size has been found to affect program Vt distribution. Devices built with newer, smaller feature sizes are expected to have slightly more sensitivity to a given X-ray inspection
when compared to older technology devices. However, sensitivity difference from one feature size to the next is very small compared to the other effects noted above.

4.3 Risk Assessment

Evaluations have shown that any X-ray exposure results in a negative shift in programmed Vt distributions. It is difficult to assess the impact on programmed bit Vt distribution based on specific X-ray inspection implementations because the Vt disturb phenomenon is the result of the accumulated effects of many interactions of high energy photons (see variety of factors shown above) with individual memory cells, each with unique physical characteristics resulting from natural semiconductor process variation. As a result, to ensure maximum data integrity for programmed bits, X-ray exposure after programming should be avoided or at least minimized (see Spansion Recommended Mitigation Measures).

Where it is deemed necessary to perform X-ray inspection, programming and X-ray inspection methodology should be carefully considered to minimize the probability of significant programmed Vt disturbance which could result in a read data error.

After September 11, 2001, the inspection frequency and intensity for all shipping methods increased including X-ray inspections. However, airport X-ray inspection systems use energies typically outside the 2-9 keV range and exposure time is short enough such that the amount of absorbed energy, or dose, is low. Survey results from monitored Spansion shipping routes indicated that the X-ray exposure dose for hand-carry baggage airport inspection is at less than 50 mRad (Radiation Absorbed Dose), while checked baggage could be subjected to higher doses of 300 mRad typical. This can be compared to assembly line X-ray inspection methods that can result in doses on the order of Rads. The conditions (X-ray tube voltage, current and the distance to the samples) used by airport inspection systems are much more moderate compared to the equipment used for inspecting the solder connections on IC devices. As a result, the impact on device functionality from airport inspection is typically at no or minimum risk.

4.4 Spansion Recommended Mitigation Measures

A variety of control methods should be considered, including:

1. Using a 300 µm thick Zn filter is the most effective method to reduce X-ray impact. A thin zinc filter is a useful agent to absorb very soft X-rays to which silicon is particularly vulnerable, yet transmit soft and medium energy X-rays required to obtain good X-ray images during solder connections inspection. Zinc foil can be integrated with the inspection “carrier” or put between the X-ray source and the flash devices to be inspected. AMD® was issued a patent (free usage is encouraged) for the use of zinc filtering that enables X-ray inspection users to protect the IC devices from the damage effects of soft X-rays (enter 6,751,294 into http://www.freepatentsonline.com to get full text PDF for this patent).

The use of a 1 mm aluminum filter has also been proven effective in reducing negative affects on programmed Vt. Commonly used X-ray equipment filters made of Beryllium, Copper, and Stainless Steel have been proven ineffective in mitigating the damaging effects of soft X-rays.

2. Using the smallest KVpeak possible that still produces adequate images, recommending near 50 KVpeak rather than 80-110 KVpeak. This action reduces number of bits affected by 5-fold (for 50 vs. 110 KVpeak) and threshold voltage change by 2-fold. Some laminography inspection machines do not have adjustable KVpeak and the fixed KV value is large (up to 160 KV), so this could increase the risk of read data error on flash memory devices.

3. Using the smallest X-ray tube current possible that still produces adequate images, recommending near (or smaller than) 20 µA rather than traditional 40 µA. This action reduces number of bits affected by 2-fold and threshold voltage change by 1.4-fold.

4. Use as a large a distance as possible between the X-ray tube and the sample being inspected. X-ray dose varies inversely with distance. In addition be aware of collateral damage (X-ray dose in this case) due to exposure of devices not being inspected. Unintentional exposure of surrounding devices in systems with uncollimated beams could result in ten times the dose of a single inspection image.

5. Use the shortest inspection time possible, preferably on a sampling basis rather than 100%. If X-ray inspection is used after Surface Mount Technology (soldering components to Printed Circuit
Boards), refresh data, i.e. program the same data again in system without erasure for floating gate devices, but erase and reprogram for MirrorBit devices.

4.5 Summary

Evaluations have shown that any X-ray exposure to programmed flash memory will result in an undesirable shift in programmed bit threshold voltages, the result of which is degraded data readability and the potential for system failure. As such, X-ray exposure should be avoided where possible and minimized where avoidance is not possible.

Due to the variability in flash silicon, X-ray spectrums and X-ray equipment capabilities, it is not possible to provide specific guidelines on acceptable and unacceptable X-ray exposure criteria, e.g. maximum safe dose rate, maximum safe exposure time, etc... However in general, X-ray exposure of programmed flash should be avoided where possible and customers should limit the cumulative X-ray inspection exposure to the surface mount technology (SMT) memory devices to as small a value as possible. This minimizes the number of bits affected and the magnitude of the change to each affected bit. Optimally, the flash data should be refreshed by an in-system erase and program step following X-ray inspection.
Chapter 5
Assembly and Packaging

5.1 Spansion IC Packaging Technology

Electronic packages provide electrical interconnections between the IC and the board. Market demands ever-increasing memory densities in smaller form factors. As a result, feature sizes of flash devices are constantly shrinking, resulting in increased number of transistors being packed into the device. Therefore, Electronic packages need to be flexible to accommodate tighter bond pitches.

Spansion has enabling technologies to provide solutions for multi-die stacking as well as high reliability solutions required for the automotive and embedded infrastructure. Multi-Chip Packages (MCP) have been widely adopted as a viable solution to meet market trend of increasing functionality in smaller footprints, requiring advances chip stacking technology.

Spansion provides a wide variety of packages to meet customer’s needs. They include conventional lead-frame packages such as TSOP, SOIC, WSON, PQFP as well as laminate-based BGA packages for both single chip and MCP. Packages are co-designed with silicon for optimal electrical, thermal and long-term mechanical reliability requirements.

Spansion offers standardized electrical footprints and package body sizes to meet customer requirements for quick time-to-market and product flexibility so that changing memory types and densities can be implemented without changes to PCB design.

5.2 Pb-free/Green Package Solutions

Pb-Free packages are Spansion’s standard offerings and they are compliant with RoHS. Since certain industries have received exemptions from the RoHS directive, Spansion also supports RoHS 5/6 products which contain SnPb solder while developing a plan with customers for a full conversion to lead free in early 2011. Spansion’s lead-free material set has the following characteristics:

- Cu (Copper) leadframe packages - 100% matte Sn (Tin) plating.
- Laminate packages - Solder balls composed of SnAgCu.

Spansion is fully committed to protect our environment and offers green packages that do not contain substance that have been identified as harmful to the environment. The maximum trace amounts of Halogen substances allowable in Spansion’s green packages are listed below.

- Chlorine: <900 ppm
- Bromine: <900 ppm
- Total concentration of Chlorine and Bromine: <1500 ppm

For more information about Spansion’s Pb-free/Green package solutions, please refer to the following spansion web sites:

- Pb-free packages from Spansion
- Packaging material
■ Declaration of compliance with customer requirements for low-halogen products

Moving from PbSn to Pb-free assembly will subject the customer’s PCB and associated components to higher reflow temperatures. It is recommended to maintain excellent reflow furnace peak temperature and dwell time process control to avoid unnecessary thermal exposure. Higher temperatures can lead to greater warpage and movement as reflow temperatures exceed the glass transition temperature of many of the plastic materials used commonly in semiconductor packaging and board technologies. Similarly higher temperature require greater diligence with respect to moisture sensitivity ratings and storage conditions of semiconductor components with which the reader will be come familiar in the next sections.

5.3 Moisture Sensitivity

Plastic packages and many of the materials they use are capable of absorbing moisture when placed in an environment with a relative humidity (RH) greater than 0%. The pressure of this moisture, absorbed as vapor, increases dramatically when the package is exposed to high temperatures of a typical reflow (with peak temperatures around 210-260°C). As the moisture rapidly leaves the packages, inherent weaknesses in the package or materials may result in delamination (separation along the interface between two dissimilar materials) or cracking (separation within the bulk material of one or more materials). These phenomena can result in a variety of failure modes, such as substrate trace cracking, external package separation, bond wire lifting, and die cracking. In some instances, the pressure within the package is so severe and may result in what is commonly known as “popcorning,” as the package bulges physically, separating and cracking the package, due to the rapid egress of the water vapor. Often times, a “popping” sound can also be heard as the moisture laden parts go through reflow. To adequately understand a part’s classification with respect to moisture sensitivity, Spansion performs testing and classification in accordance with IPC/JEDEC J-STD-020 (Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices (SMD), the latest version being D.1 (March 2008) as of the time of this document. In addition to the J-STD020 specification, there also exists JEITA EIAJ ED-4701/301 (Resistance to Soldering Heat - Surface Mounting Devices) specifying a similar process to which Spansion is also compliant.

Also known as “Preconditioning,” this testing is performed designed to simulate the dry bake, transport, moisture bag penetration, and reflow process per the customer’s surface mount procedures. As board assemblers are apt to rework boards filled with expensive components several times, multiple exposures to the assembly heating process are required. Preconditioning consists of first baking the packages to simulate the dry bake procedure performed after electrical test, soaking the package in a moist environment at an elevated temperature followed by three cycles of either vapor phase reflow or IR/convection temperature exposure. The corresponding process flows are demonstrated by the diagram. The exact parameters for preconditioning are determined by the moisture sensitivity level of the package being tested.
The Moisture Sensitivity Classification of the part is dependent on two factors: the soak conditions (from which the Moisture Sensitivity Level (MSL) is determined) and the reflow conditions (from which the peak reflow temperature is determined). In terms of soak conditions, most SMDs in industry are classified at Jedecl MSL 3, meaning that the soak is performed at 30°C, 60%RH for 192 hours. This results in a 168h (7 day) “out of bag” time, meaning that the moisture barrier bag (MBB) can be opened and the parts can be exposed to ambient conditions for up to seven days before being reflowed. However, in order to ensure that both JEITA EIAJ standards are considered, Spansion performs a special MSL classification, as demonstrated in the table below. This special MSL, nicknamed “FMSL,” is intended not only to comply with JEDEC standards but also with JEITA standards. In addition, it allows for an extra day of time out of bag before reflow. Certain products may also be qualified to alternate JEDEC Levels or JEITA Ranks; for these, refer to the governing JEDEC and JEITA specifications mentioned above.

<table>
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<th>Standard</th>
<th>Soak Condition</th>
<th>Soak Time</th>
<th>Out of Bag</th>
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<td>30°C/60%RH</td>
<td>192 hours</td>
<td>7 Days</td>
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<tr>
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<td>30°C/70%RH</td>
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<td>30°C/70%RH</td>
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<td>8 Days</td>
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</tbody>
</table>

In terms of reflow conditions, most parts are qualified per the reflow profile attached below, and to 260°C, unless otherwise specified. The specifics of the of the reflow profile are also attached, and are obtained from J-STD-020. The profile is actually the Pb (Lead)-Free profile in the J-STD-020, but is used for all Spansion products, irrespective of their Pb content.
Once three cycles of reflow are performed (typically the first simulates board mount, the second double sided assembly, and the third rework), the parts are inspected both visually and through SAM, and then electrically tested. If they pass all criteria, they are considered to be qualified to the respective Level/Rank that was tested.

5.4 Storage of Semiconductor Products

5.4.1 Storage of Wafer and Die

Care should be taken in receiving, storing, packing, and shipping of semiconductor devices to prevent mechanical and/or electrical damage. Packaged units have an extra level of protection by virtue of the package itself. Die and wafer products require particular precautions when subjected to normal handling, shipping and storage conditions. All packaging materials should be either conductive or antistatic, including waffle pack, reels, bags, and fillers. Appropriate ESD precautions must be taken (see JESD625 or elsewhere in this document). Dry bagging or vacuum bagging of product at any point up to and including shipment to the end user should follow industry standard specifications. This includes re-baking and re-bagging of parts when necessary. The distributor or user is responsible for verifying conformance to all of the receiving, storing, packing, and shipping requirements prior to use by the end customer. When several lots of the same part number and package type exist in inventory, product should be used based upon the first-in, first-out (FIFO) inventory method (i.e., delivery or use based upon the oldest date code first).

It is possible that while in storage, especially if not being stored in a controlled atmosphere, moisture may have permeated the vacuum sealed bag that encloses the product and protects it from moisture. Although wafers and die are not inherently moisture sensitive, the moisture ingress may accelerate failure mechanisms which may only present themselves during product packaging in the form of bonding issues and delamination.

5.4.1.1 Die Topside Contamination

It is possible, over time or due to improper storage for foreign agents to contaminate the top surface of wafers or bond pads. This could result in issues such as Non-Stick-On-Pad (NSOP), topside delamination, or other such issues during assembly and packaging procedures. Tests to monitor surface cleanliness and adhesion (water droplet, for example) should be performed, and plasma cleaning should be implemented in the assembly process if necessary. Spansion also recommends a limited trial-run or assembly evaluation to guarantee favorable results before the product is placed into mass-production.
5.4.1.2 Improper Storage Conditions
If die and wafers are not stored properly, then issues like those mentioned above could have an even greater probability of occurrence. Spansion always recommends that wafers be kept in an environmentally controlled area and in proper containers and vacuum sealed, if possible. Wafers that are not vacuum sealed must be placed in a Nitrogen (N2) purge cabinet with a flow rate of 2 to 6 SCFH (Standard Cubic Feet per Hour). In an environmentally controlled area, FED STD 209 Class 1000/ISO 14644-1 Class 6 or below, wafers may be stored in open containers while in the queue for testing or while processing is in progress. Wafers may be transported in individual wafer carriers without benefit of a top cover provided the area is Class 1000/ISO Class 6 or below, however, when not in use, it is always recommended for the wafer contained to retain its cover.

5.4.1.3 Risk with KGD Parts
KGD Parts are normally shipped in tape and reel, and it is more difficult to ensure long term reliability because of the nature of the transport medium. For very long term storage, it is recommended that products be purchased in wafer form.

5.4.1.4 ESDS Considerations
The system for electrostatic discharge sensitive (ESDS) protection should be in compliance with JESD625. When removing devices from reels, the cover tape should be removed at a rate of 10 mm/second or less, and at an angle of between 165° and 180° from the embossed carrier tape to minimize electrostatic generation.

In general, the quality and reliability of long term stored Semiconductor IC wafer and die product should be acceptable and comparable to newer product. However, to ensure that no issue will be observed in assembly, Spansion recommends an evaluation of long term stored product before mass production is initiated. It is recommended to purchase these products for long term storage in wafer form.

Spansion's own internal specifications allow for wafer storage of up to five years. However, Spansion can make no guarantees on wafers that are stored outside of its own die banks and/or holding locations. In general, parts could still be used after this five year limit has passed, but it is recommended that a disposition procedure ensuring the good manufacturability of these wafers be followed.

5.4.2 Storage of Packaged Semiconductors
In general, the same concerns apply to packaged product in terms of ESD precautions and FIFO, as mentioned in the section on wafer and die IC products. However, packaged products have inherently different failure mechanisms and these are discussed below.

5.4.2.1 Moisture Barrier Bag Penetration
It is possible that while in storage, moisture may have permeated the sealed moisture barrier bag (MBB) that encloses the product and protects it from moisture. If, after opening the MBB, the humidity indicator card has changed color showing that moisture has penetrated the MBB and bake is required, the parts must be baked per the recommended conditions shown on the label adhered at the MBB bag before they are used. If possible, the baked parts should be placed in a sealed bag as well before use.

5.4.2.2 Oxidation/Discoloration on Leadframe-based Packages
In rare instances, while in extended storage, the leads on leadframe-based packages such as TSOP or SOIC products may discolor and/or oxidize. Cleaning fluxes should be employed to ensure proper cleaning and best adhesion to the board. Solderability testing should be performed in order to ensure good solder wetting. Spansion also recommends a limited trial-run or assembly evaluation to guarantee favorable results before the product is placed into mass-production.
5.4.2.3 Oxidation/Discoloration on Substrate-Based Packages (BGA)

In the same way that leadframe-based packages can oxidize and/or discolor, in rare circumstances the solder spheres attached to the underside of substrate-based packages may also discolor and/or oxidize. As with leadframe packages, BGA packages should be treated in a similar fashion to ensure good results with assembly.

5.4.2.4 Difficulty with Packaged Parts Shipped in Tape and Reel

When packaged parts are shipped in tape and reel, it is more difficult to ensure long term reliability because of the nature of the transport medium. Tape and reels, although packaged in a moisture barrier bag, may still experience some moisture ingress, and as a result, the parts inside may need to be baked. However, reels cannot withstand the higher temperatures required for dry bake, and the parts must be placed into trays, which can withstand baking temperatures. For very long term storage, it is recommended that products be purchased in trays so that any necessary bake can be performed easily.

5.4.2.5 ESDS Considerations

The system for electrostatic discharge sensitive (ESDS) protection should be in compliance with JESD625. When removing devices from reels, the cover tape should be removed at a rate of 10 mm/second or less, and at an angle of between 165° and 180° from the carrier tape to minimize electrostatic generation.

Just as for wafer and die product, the general quality and reliability of long term stored semiconductor packaged IC product should be acceptable and comparable to newer product. However, to ensure that no issue will be observed in assembly (board mounting), Spansion recommends an evaluation of long term stored product before mass production is initiated.

5.5 ESD Concerns

Semiconductor devices are inherently sensitive to electrostatic discharge (ESD). Special precautions need to be taken inside the factory and when handling these components in order to ensure that no ESD damage occurs to the parts while they are being assembled or mounted. In general, all equipment, machinery, and personnel that handle semiconductor equipment must be guarded against ESD events. The main details and requirements are listed in detail in JEDEC JESD625-A. It gives minimum requirements for ESD protected workstations, tools and areas, as well as grounding considerations, ESD packaging requirements for ESD Sensitive (ESDS) devices, compliance verification, ESD handling training, and best methods for minimizing static charge. As the final section is the most relevant, its content is summarized here.

Static charge preventive actions shall be utilized at ESD protected areas and workstations where electrostatic potentials greater than ±1000 volts ARE measured AND unprotected ESDS devices are within twelve (12) inches of the charged sources. Charge prevention/neutralization methods include, but are not limited to, antistatic solution treatments, relative humidity control, air ionizers, sleeve protectors, and ESD protective clothing.

**Antistatic solution** – Antistatic chemicals (antistat solutions) can be used to prevent static charge generation on static generating/charging materials in the work or storage areas. During application of any antistatic chemical, the user must consider the following:

- The antistatic solutions should be chosen to avoid contamination of ESDS devices.
- Antistatic spray or solutions must not be applied in any form to energized electrical parts, assemblies, panels, or equipment.
- Antistatic solutions should not be applied when devices and/or packages are at risk of direct exposure to spray mists.
- The need for initial application and frequency of reapplication can only be established through routine electrostatic field measurements during normal operations using an electrostatic fieldmeter.

Relative humidity control - Relative humidity has a significant impact on the generation of static electricity and its control is recommended where practiceable.

**Note:** The recommended minimum humidity is 40% R.H.

**Air ionizers** – Air ionizers, when used, shall conform to the following:
Table ionizers shall be positioned so that the devices at the ESD-protected workstations are within the ionizer manufacturer's specified coverage area. The ionizer shall be aimed at the devices and operator's hands rather than at the operator.

Ceiling ionizers shall be oriented in relation to the work surfaces in accordance with the ionizer manufacturer's instructions.

Devices shall not be brought closer to the ionizer than specified by the ionizer manufacturer.

There shall be an unrestricted, straight line air flow between the ionizers and the unprotected devices.

Ionizer balance (positive and negative ions) shall be verified per table 2.

Ionizer charge decay performance shall be verified using the method described in EOS/ESD-S3.1 per table 2.

ESD protective smocks, when worn, shall accomplish the following:

The ESD protective smocks shall be buttoned (except for the collar) whenever the wearer is at an ESD protected workstation or in a designated ESD protected area.

The ESD protective smock manufacturer's cleaning instructions should be followed to gain maximum effectiveness and utility from the smocks.

Gloves/finger cots - When gloves or finger cots are required, only cotton gloves, antistatic/conductive gloves, or antistatic/conductive finger cots should be used when handling ESDS devices.

In summary, care should be taken to protect these devices from ESD using proper precautions (as outlined in JEDEC JESD625-A) to avoid any unintended ESD events.

5.6 Pack and Ship

Introduction
Spansion provides information on its packages and packing methodologies through its Packing and Packaging Handbook. The handbook, accessed through the link below, includes information on the integrated standard packing methodologies for Spansion packages (see http://www.spansion.com/Support/TechnicalDocuments/Pages/Packaging.aspx).

5.6.1 Trays

Trays are used instead of tubes to protect higher lead/ball count packages from electrical and mechanical damage during handling and shipment. Trays are also suitable for product presentation to board assembly equipment. As standard practice, single-chip FBGA packages and multi-chip packages (MCPs), as well as PQFP, SSOP, TSOP, USON, and WSON packages are shipped in trays. Some leadframe packages such as SOIC and PLCC are shipped in tubes as a standard with the option of shipping in trays.

All trays are uniformly sized, in compliance with standard JEDEC outlines. As much as possible, trays that are made of 25 percent recycled material are procured for use in the shipment of Spansion products. The fiber tray material is either carbon-filled or antistatically coated to provide ESD protection. The trays are made of static dissipative polysulfone material, or equivalent. The temperature at which each tray can withstand continuous operation varies. See the notes section of each tray dimension drawing for specific information.

Typically, packages are placed in the trays so that the device pin one is oriented to the notched corner of the tray, which enables pick-and-place equipment setups to be compatible for all packages and leadcounts. However, with certain package constructions, the device pin one is oriented at the upper right, opposite of the notched corner of the tray.
5.6.2 Tube

Tube packing is available for PDIP, PLCC, SOIC, USON and WSON packages. Tubes are made of antistatic coated PVC to protect the product from electrical and mechanical damage.

Packages are loaded into tubes with each package uniformly oriented, please refer to the Packing and Packaging Handbook for the orientation of specific package. The end-plugs, made of antistatic material, secures the packages in the tube and helps minimize excessive movement of packages during shipping and handling.

5.6.3 Tape and Reel

Spansion is also offering products in Tape and Reel in addition to the standard packing in trays. This packing option is available for all packages except PDIP. This packing method is suitable for the large quantity usage that minimizes machine change over time.

The Tape and Reel consists of a pocketed carrier tape sealed with a protective cover tape to hold the products and are wound onto a plastic reel. Sprocket holes along the edge of the carrier tape enable direct feeding into automated board assembly machine. The pocketed carrier tape is made of a carbon loaded static dissipative polystyrene material or equivalent with a surface resistivity level >1 x 10^5 and < 1 x 10^12 ohms per square.

Typically, packages are placed in the tape pocket so that the pin one is oriented to the sprocket hole.

5.6.4 Other

Wafer Jar

Wafer jar is the standard carrier for fabricated wafers. Wafers are packed in a wafer jar that is made of conductive polypropylene.

Waffle Pack

Waffle Pack is a carrier for singulated die. The waffle pack is made of conductive, polypropylene material that provides static protection. The quantity of pockets per waffle pack varies depending on the die size. The die are placed in each pocket and uniformly oriented.

Surftape and Reel

Surftape and Reel is another packing option for shipping singulated die. It is a benefit for high volume, automated board assembly operation. Surftape consists of a conductive, polystyrene tape with windows punched in it to create a slight recessed pocket. Two strips of sticky tape backside are attached along two sides of the window. A sticky tape has a pressure-sensitive coating which holds each die in place. Each die is loaded into the surftape with device pin one is oriented to the top of the pocket.

For more information about pack and ship, please refer to the Packing and Packaging Handbook.
5.7 Package Thermal Characteristics

5.7.1 Introduction

Flash memory devices consume much less power than most other memory devices. The level of power consumption in worst case scenario is around 100 mW. Therefore thermal management in most flash applications is not critical. However, due to the low power consumption, estimation of junction temperature is different from ASIC devices whose power consumption is significantly higher than flash memory devices.

5.7.2 Package Thermal Resistances and Thermal Characterization Parameters

There are various terms used to represent the thermal heat flow out of conventional plastic packages in the industry today. Thermal resistance values are useful in comparing different types of packages but are generally inadequate in estimating junction temperature in the user's application. Thermal characterization parameters can be applied to estimate component junction temperature in customer's applications. Junction temperature needs to be maintained under a specified limit (device technology dependent) to ensure proper device functionality and reliability. We will discuss the following thermal parameters in this section: $\theta_{JA}$, $\Psi_{JT}$, and $\Psi_{JB}$.

$\theta_{JA}$ is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure as described in JEDEC document JESD51-2. There are many factors that affect $\theta_{JA}$ such as die size, package design, packaging material, PCB dimension, number of layers, and metal content, to name a few. Simulation shows that under natural convection for many plastic packages, the majority of the power is dissipated through the PCB to the ambient environment. Therefore, it is important to note that $\theta_{JA}$ heavily depends upon the system design. Figure 5-3 shows how the PCB design affects $\theta_{JA}$. JEDS51-2 defines the experimental setup for measuring $\theta_{JA}$. $\theta_{JA}$ and other thermal resistance values, in most cases, should not be used to estimate how a package will perform in a specific application due to the fact that these values are measured under standardized test conditions that do not match the user's application conditions.

![Figure 5-3. $\theta_{JA}$ vs. PCB Size](image)

Notes:
1. The results are from numerical simulation using FBGA48 package.
2. PCB type is 2s2p (2 signal layer + 2 power layer).

The reader may also have heard the term $\theta_{JC}$, or junction-to-case thermal resistance. This parameter is often misused and actually stems from ceramic packaging where the outside surface of the package or case was/is properly heat sunk. In such cases there is a single primary package heat transfer path. This is not the case with most plastic packages, and is not the case with low power Spansion flash plastic packages. With multiple heat transfer paths, thermal characterization parameters can be used to estimate silicon junction temperatures.

$\Psi$ is the junction-to-top thermal characterization parameter where $Tt$ is the temperature measured at the top center of the package as described in JEDEC documents JESD51-2 and JESD51-6. As mentioned, with regard to plastic packages there are multiple thermal pathways and various boundary condition temperatures that may be measured by the customer in their system. The user can apply $\Psi_{JT}$ equations, which will be reviewed in the next section, to estimate the component junction temperature in their specific application by measuring the temperature at the top center of the package during system operation.
Similarly, $\Psi_{JB}$ is the junction-to-board thermal characterization parameter where the board temperature, $T_b$, is measured in the actual application on a metal trace within 1 mm of the packaged flash device. The power dissipated by the flash chip may leave the package through any thermal path or combination of paths when using $\Psi_{JB}$ or $\Psi_{JT}$ with the respective boundary condition temperature measured.

Spansion flash memory is typically not the highest power device on a customer's board. As a result, nearby, higher power devices may actually heat the flash device. $\Theta_{JA}$ values by definition apply to single component situations within a controlled test environment. Thermal characterization parameters like $\Psi_{JT}$ and $\Psi_{JB}$ make use of application-specific temperature measurements and more accurately can be used to estimate flash silicon junction temperature. If there is a need to more accurately predict the thermal performance of a component in the user's system, finite element models (FEM) and computational fluid dynamics can be used for comprehensive simulations. Generally system level thermal simulations are the user's responsibility but Spansion as a component supplier can act as consultants or actively assist in thermal simulations. Please contact your local representative for further information regarding system level simulation.

### 5.7.3 Estimating Junction Temperature

Table 5-1 can be used to calculate junction temperature $T_j$ from the definition of the thermal parameters and a measured boundary condition temperature in the system.

**Table 5-1. Junction Temperature Equations**

<table>
<thead>
<tr>
<th>Measured Boundary Condition</th>
<th>Thermal Parameter to use</th>
<th>Junction Temperature Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_b$</td>
<td>$\Psi_{JB}$</td>
<td>$T_j = T_b + \Psi_{JB} \times P$</td>
</tr>
<tr>
<td>$T_t$</td>
<td>$\Psi_{JT}$</td>
<td>$T_j = T_t + \Psi_{JT} \times P$</td>
</tr>
<tr>
<td>$T_a$</td>
<td>$\Theta_{JA}$</td>
<td>$T_j = T_a + \Theta_{JA} \times P$</td>
</tr>
</tbody>
</table>

**Note:**
1. Junction temperature under defined test conditions

Definition of terms

$T_j =$ junction temperature, defined as the maximum temperature on the die. Unit: °C.

$T_a =$ ambient temperature, defined as the temperature of “still air” in a one cubic foot sealed test enclosure. Unit: °C.

$T_t =$ top center temperature of packaged flash unit in customer’s board. Unit: °C.

$T_b =$ PCB surface temperature measured on a lead foot of a leadframe package or on a board trace within 1 mm of the ball grid array (BGA) packaged device in customer’s board. Unit: °C

$P$(watts) = The total power (heat) dissipated in the flash device = $I$ (amps) x $V$ (volts).

Example using $\Psi_{JB}$: The flash device inside a WSON package is operating at a max power consumption of 50 mW. The PCB temperature is measured to be 50°C on a board trace near the flash package. The $\Psi_{JB}$ of the package is 2 C/W. The junction temperature of the device is estimated to be 50.1°C ($50 + 0.05 \times 2$).

Example using $\Psi_{JT}$: The flash device inside a TSOP package is operating at a max power consumption of 50 mW. The package top center temperature is measured to be 85°C. The $\Psi_{JT}$ of the package is 5 C/W. The maximum junction temperature of the device is estimated to be 85.25°C ($85 + 0.05 \times 5$).

In conclusion, the customer may obtain $\Psi_{JB}$, $\Psi_{JT}$, and $\Theta_{JA}$ values for any Spansion devices and packages by contacting your local representative. The thermal characterization parameters, $\Psi_{JB}$ and $\Psi_{JT}$, are used to approximate the three dimensional heat flow characteristics of plastic packages using the measured boundary conditions listed above. If more accurate calculations for junction temperature are needed thermal simulations must be conducted to estimate the flash junction temperature.
5.8 Surface Mount Guidelines

5.8.1 Introduction

Due to high demand for electronic products offering smaller size and higher mounting densities, there has been a shift in IC mounting methods from traditional through-hole mounting to surface mounting. Spansion provides a wide variety of surface mounted packages, which could be categorized as:

- Lead type packages with gull wing lead
- Leadless type packages with flat contact to PCB
- Ball grid array type packages

In order to achieve high PCB assembly yield and strong solder joint, many factors should be taken into consideration. This section provides general guidelines of PCB design, stencil design, and solder paste/reflow profile selection.

5.8.2 Recommended PCB Land Pad Size and Stencil Design Guidelines

PCB assembly yield could be greatly influenced by the PCB land pad design. The examples of recommended PCB land pad size for leaded and leadless type packages as well as stencil design guidelines are described in the Application Notes Section of the Spansion Packaging Handbook. The recommendations are based on IPC (Institute for Interconnecting and Packaging Electronic Circuits) Generic Requirements for Surface Mount Design and Land Pattern Standards: IPC-7351A.

Additional information can be obtained from your local representative or on the web at: http://www.spansion.com/Support/TechnicalDocuments/Pages/Packaging.aspx

5.8.3 Solder Paste and Reflow Profile

Spansion usually provides packages with a low stand-off height and small terminal pitch, a no-clean, type-3 solder paste is recommended. Sn63/Pb37 (63%Sn, 37%Pb) alloy is recommended for standard eutectic solder paste and SnAgCu alloy is recommended for lead-free application.

The actual reflow profile depends on the thermal mass of the entire populated board and the solder pasted used. Most paste manufacturers provide a suggested thermal profile for their products. Also customers should optimize their board mounting reflow profiles per their board design. However, internal studies have shown good results when using the following general reflow guidelines:

For SnPb Paste: The reflow peak temperature should be kept in the 220-230°C range, with total time above 183°C for 30-60 seconds, and ramp down rate at -5°C/second maximum. An actual reflow profile used to produce good board level reliability result is shown in Figure 5-4.

For SnAgCu Paste: the reflow peak temperature should be kept in the 235-245°C range, with total time above 217°C for 30-60 seconds, and ramp down rate at -5°C/second maximum. An actual reflow profile used to produce good board level reliability result is shown in Figure 5-5.

Figure 5-4. SnPb Reflow Profile with Dwell Time Above 183°C = 50 sec and Peak Temperature= 222°C
5.8.4 Rework Procedure Considerations and Returning of Failing Units for Failure Analysis

Rework procedures must include precautions to ensure that the physical and electrical integrity of the device is not affected adversely.

Overheating during package extraction or remounting could result in package-related delamination and die cracking. Excessive heat applied to a device can also cause data corruption and data loss. Using sharp objects such as a razor blade or applied mechanical force can cause package-related damage and die cracking.

For the reasons stated above, Spansion recommends that customers return surface mounted failing units that require failure analysis at Spansion with the PCB if possible for extraction at Spansion.
Chapter 6

Manufacturing Flow

6.1 Introduction

Considering the effects of various environmental factors and manufacturing processes can have on programmed flash devices, Spansion has constructed a preferred board assembly manufacturing flow. Board assembly can require various thermal cycles and inspection techniques that have been discussed in earlier chapters of this User's Guide and can have effects on stored data, corrupting that data or at the extreme, damaging the memory device. The steps and the sequence of those steps in this flow have been derived from discussions with a variety of customers across a breadth of markets that use Spansion flash memory products in their applications. The objective of the recommended sequence is to limit damaging effects of thermal exposure and inspection techniques. To ensure data integrity it is best practice to perform verifications after programming. In the case of manufacturing assembly and system performance verification procedures, it is recommended that only that programming necessary for functional test be done early in the board assembly process. Final programming is then done after system verification and at the end of the manufacturing assembly flow minimizing the influence of manufacturing stresses on non-volatile data. With these measures data integrity can be preserved and data accuracy verified before system operation.
### Process Step

<table>
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<td>High Speed Placement</td>
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<td>Reflow</td>
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<td>Solder Inspection</td>
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<tr>
<td>Board Inspection</td>
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<tr>
<td>Stencil</td>
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<tr>
<td>High Speed Placement</td>
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<td>Precision Placement</td>
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<td>Reflow</td>
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<tr>
<td>Solder Inspection</td>
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<td>Wave Solder</td>
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<table>
<thead>
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<th>Board Verification</th>
<th>Second Side</th>
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<tbody>
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<td>ICT</td>
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<td>Functional Test</td>
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<td>Board Mounting into system</td>
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<table>
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<tr>
<th>System Installation</th>
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<td>Functional test</td>
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<table>
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<th>System Verification</th>
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### Comments

- **Visual Inspection**
- **Solder Paste Stencil**
- **Placement of smaller components**
- **Recommended for flash component to be placed on second side to minimize thermal exposure**
  - Adhere to Spansion / Jede spec J-STD-020D.01
  - Use Boundary Scan /in-circuit testing (ICT), Where Xray is needed refer to Chapter 4
- **Visual Inspection**
- **Solder Paste Stencil**
- **Placement of smaller components**
- **Recommended for flash component to be placed on this side to minimize thermal exposures**
  - Adhere to Spansion / Jede spec J-STD-020D.01
  - Use Boundary Scan / ICT, Where Xray is needed refer to Chapter 4
- **Check Lead Integrity**
  - Recommend at this stage to do checksum on flash to ensure data is correct. Use different Vcc where possible.
  - Installation of mainboard into system
  - Installation of power supply, monitor, i/o, etc
  - Inspection of completed system
  - System Boot up test, where possible do a full Check sum verification of just a simple boot test.
  - Functional test should ensure that flash can be accessed correctly (ID Check, read, write/erase)
  - Where possible perform test at corner conditions.
  - Always ensure full flash verification at this step.
  - It is recommended that the flash be thoroughly verified and reprogrammed where needed.
  - It is recommended that the majority of programming be done at the end of the assembly flow.
Colophon

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