

Quarterly Reliability Report

Q1 2012

Data by Process Technology



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1. Introduction

Spansion's Qualification Maintenance Program (QMP) is used to measure the reliability of all process technologies on a regular basis. This is an extensive effort that is aimed at providing generic fab process coverage for all fab process technologies. Typically about 20,000 devices per month are subjected to a battery of reliability stress tests.

The Qualification Maintenance Program has two purposes:

1. Improved Reliability Performance

Each reject is analyzed to its root cause in order to drive continuous improvement through the implementation of corrective actions.

2. Generation of Reliability Data

QMP test results are used to assess the benefits of burn-in, provide estimates of typical lifetimes, model field applications, and determine suitability of plastic packaging in various temperature and humidity environments.

Qualification maintenance testing is conducted on representative samples of devices from each process technology. Sampling is not limited to process technologies from in-house wafer fabs but also includes Spansion certified external foundries. Devices are selected on the basis of complexity, production volume and strategic importance. Process, package and product reliability qualification determine device selection.

A number of process technology groupings are established for the purpose of reliability assessment. These groupings result in larger sample sizes so that the reliability analysis is statistically significant. Process similarity guidelines are used to define these process groupings.

2. QMP Tests and Test Conditions

The results of the QMP testing for the past six quarters are summarized in this document. The stress tests employed and the typical test conditions used are shown in the [Table 2.1](#).

Table 2.1 Reliability Monitor Stress Conditions

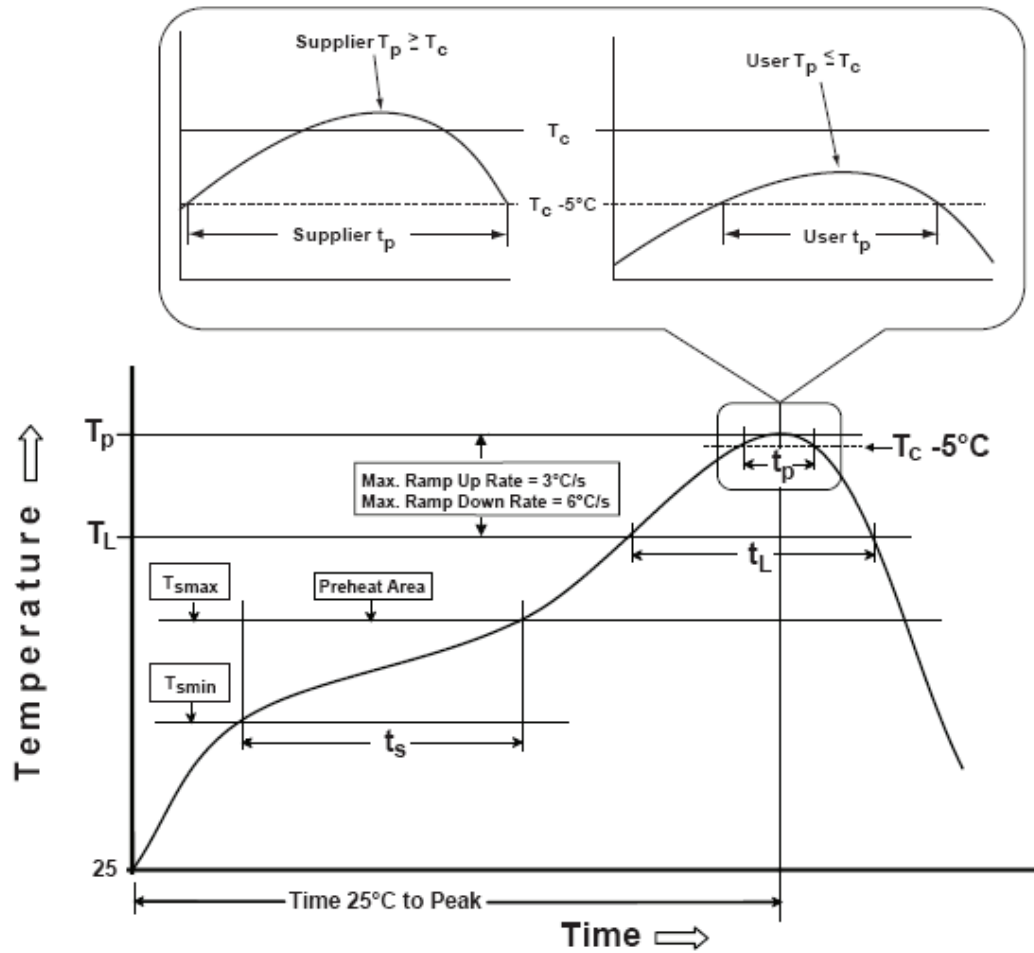
Stress	Read Points	Sample Size (Typical)	Ambient Condition
Early Life	24, 168 hours	350	150°C (1), 125°C
Inherent Life	1000 hours	120	150°C (1), 125°C
HAST	264 hours	77	110°C, 85% RH
	96 hours		130°C, 85% RH
Temperature Cycle	100, 1000 cycles	77	-40°C to 150°C
	500, 1000 cycles		-55°C to 125°C
Unbiased HAST	96 hours	77	130°C, 85% RH, no bias
Data Retention	500, 1000, 2000 hours	77	150°C

Note

1. Devices dissipating low power are life tested at 150°C.

Plastic surface mount devices are pre-conditioned prior to undergoing Temperature Cycling, Unbiased HAST, and HAST. Pre-conditioning is required in order to simulate the stresses to which the packaged parts are subjected to during shipping, storage, board assembly and cleaning operations. A convection reflow profile and the pre-conditioning flow are shown below.

Figure 2.1 Typical Convection and IR Soldering Profile



Parameter	Conditions
Preheat Temperature Range and Time	150°C 200°C for 60-120s
Ramp-up rate (TL to Tp)	3 °C/s max.
Liquidus temperature and time	217°C for 60-150 seconds
Peak package temperature (Tp)	260 °C (Unless otherwise specified)
Time (tp)* within 5 °C of Peak	30* seconds
Ramp-down rate (Tp to TL)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.

Figure 2.2 Standard Preconditioning Flow for Dry Packed Packages

Table 1
JEDEC Moisture Soak Requirements

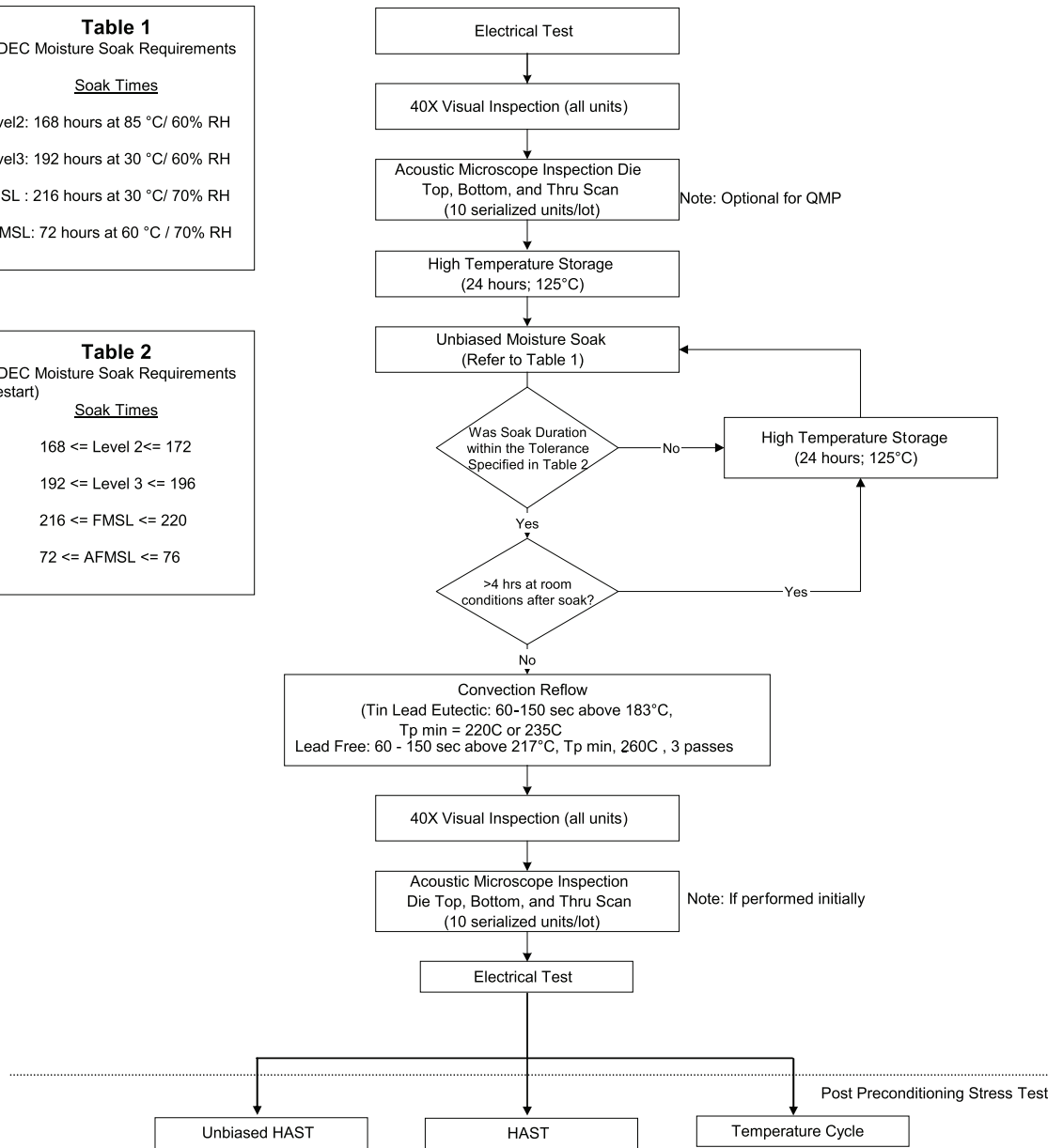
Soak Times

Level2: 168 hours at 85 °C/ 60% RH
 Level3: 192 hours at 30 °C/ 60% RH
 FMSL : 216 hours at 30 °C/ 70% RH
 AFMSL: 72 hours at 60 °C / 70% RH

Table 2
JEDEC Moisture Soak Requirements (Restart)

Soak Times

168 <= Level 2 <= 172
 192 <= Level 3 <= 196
 216 <= FMSL <= 220
 72 <= AFMSL <= 76



3. Failure Analysis

Every reject that is encountered during the course of QMP stress testing provides an opportunity for continuous improvement through identification and elimination of the root cause. Additionally, there is a significant opportunity to understand the cause of variance in products, even while they meet specifications.

Failure analysis in the semiconductor industry has evolved towards a more thorough understanding of the device physics of the underlying process technologies. Different skills, knowledge and tools are also required to analyze defects that exhibit no morphology using conventional failure analysis techniques.

Electrical failure analysis of Spansion finished products is done by three Device Analysis Laboratories located around the world. One is located in the United States, and two are located in Asia Pacific. These laboratories serve the local sites or customer base by providing analytical services on packaged devices. This includes analysis of our sub micron products from qualification stresses, reliability monitor stresses, quality test failures, customer returns, and engineering evaluations.

All of the laboratories have a complete set of tools required for analysis of the devices for which they are responsible. All laboratories have Field Emission SEMs with significantly enhanced resolution capability; Scanning Acoustic Microscopes, X-Ray capability for package evaluation and several labs have windowless EDX detectors for extended analytical capability. The laboratories in Sunnyvale and Penang have Focused Ion Beam (FIB) capability, which is used during new device debug (cutting and deposition of metal lines allowing for circuit modification) and for failure analysis where probe points can be created and micro precision cuts aid in cross sectioning.

Other tools common to all labs include automatic decapsulation capability for plastic devices, both wet chemical and dry delayering (plasma and Reactive Ion Etch), optical microscopes with cameras, mechanical probe stations to electrically examine inside the device being evaluated, laser systems for circuit isolation, and polishing wheels for die and package cross sectioning. Each lab has a Layout Tool to provide engineer access to the physical layout drawings of the device that they are evaluating.

These labs are unified by an accurate Device Analysis Database (DAD), which allows access to all failure analysis work worldwide.

Spansion is committed to providing the "state of the art" failure analysis tools necessary to assure quality products.

4. Reliability Data/Analysis

The reliability data generated from the Qualification Maintenance Program is presented in this section along with a detailed description of the modeling procedure used for estimating reliability under field conditions. Also included is a summary of environmental stress results for each process technology grouping by package types.

Average failure rates are calculated for time periods related to both early life and inherent life. The early life period corresponds to approximately the first 4,000 hours at field use conditions. The inherent life corresponds to the useful life beyond the first 4,000 hours of field operation. For these calculations, device operation temperature is assumed to be 55°C ambient. Voltage acceleration factors are used in the analysis wherever applicable.

4.1 The Exponential Distribution

The exponential distribution is simple to use, well understood and as valid as any for life tests with large sample sizes and few failures. No actual distribution can be implied as there is seldom enough data to determine one. The exponential distribution, characterized by a constant failure rate, is a special case of the Weibull. The average failure rate is the same as the instantaneous failure rate for the exponential distribution because the failure rate is constant.

The exponential distribution is the only one for which a MTTF (mean time to failure) value may easily be estimated and it is simply the reciprocal of the failure rate (λ). In addition it is the only one for which a confidence level may be readily assigned to the failure rate calculation.

The conventional expression for the failure rate, λ , is

$$\lambda = \chi^2(2n + 2, 1 - \alpha) * 10^9 / (2 * SS * t * AF)$$

where λ is the failure rate in FITs (failures per billion unit-hours), $\chi^2(2n+2, 1-\alpha)/2$ is the upper confidence value for “n” failures and upper confidence limit, (expressed as a decimal value), **SS** is the sample size, t is the test duration in hours, and **AF** is the acceleration factor relating the life test junction temperature to a assumed field junction temperature.

The χ^2 (chi square) value for 2n+2 degrees of freedom and the probability, 1- α , can be obtained from a table or calculated using Microsoft® Excel chi squared inverse function [=CHIINV(1- α ,2n+2)].

The best way to understand the concept of confidence levels is to consider this example. Assume that a life test on a 100-part sample from a certain product population had one failure and a 60% confidence level was desired. The chi square value corresponding to one failure at 60% confidence is 2.02. This means that one has a 60% confidence that the “true” value of the population's defect rate is between zero (or some very small value) and 2.02%.

4.2 Failure Distributions

The lognormal and Weibull CDF's are the distributions most often used to represent reliability failure mechanisms. The exponential distribution, characterized by a constant failure rate, is a special case of the Weibull. The lognormal distribution is specified by two parameters: T_{50} , the median time to failure, and sigma, the shape parameter. Similarly, the Weibull distribution, which can be written in closed form as

$$F(t) = 1 - \exp[-(t/c)^m],$$

is characterized by a characteristic life c and a shape parameter m. The value of the shape parameter determines whether the failure rate is increasing ($m > 1$), decreasing ($m < 1$), or constant ($m = 1$). The exponential distribution, is specified completely by the one parameter c which is called the mean time to failure (MTTF). [Figures 4.1 and 4.2](#) show failure rates for several values of the scale parameters of the lognormal and Weibull distributions, respectively.

$$F(t) = 1 - \exp[-(t/c)],$$

Figure 4.1 Lognormal Distribution

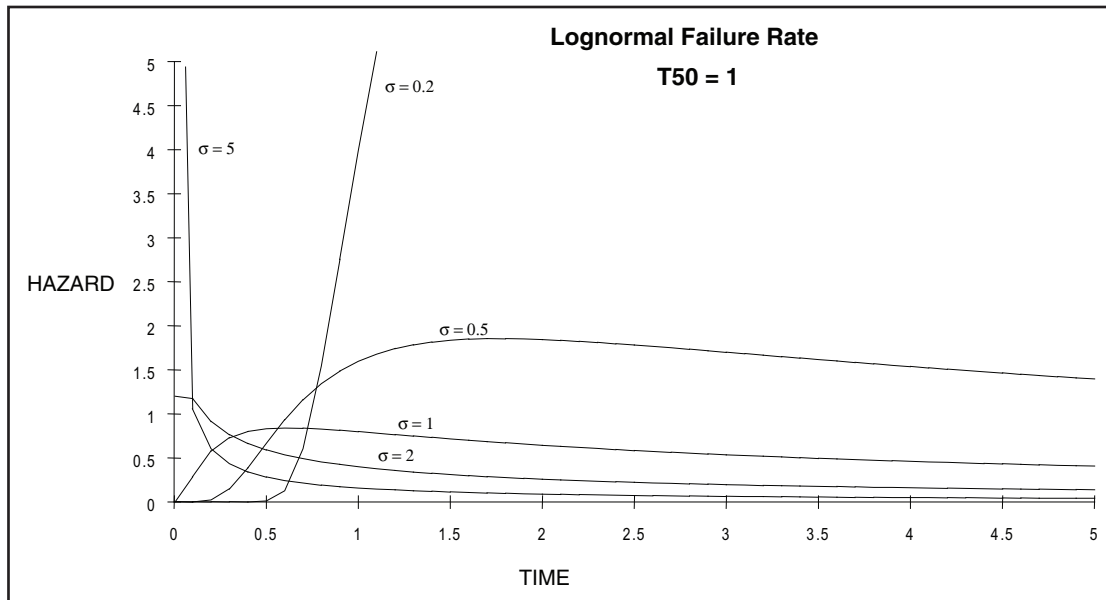
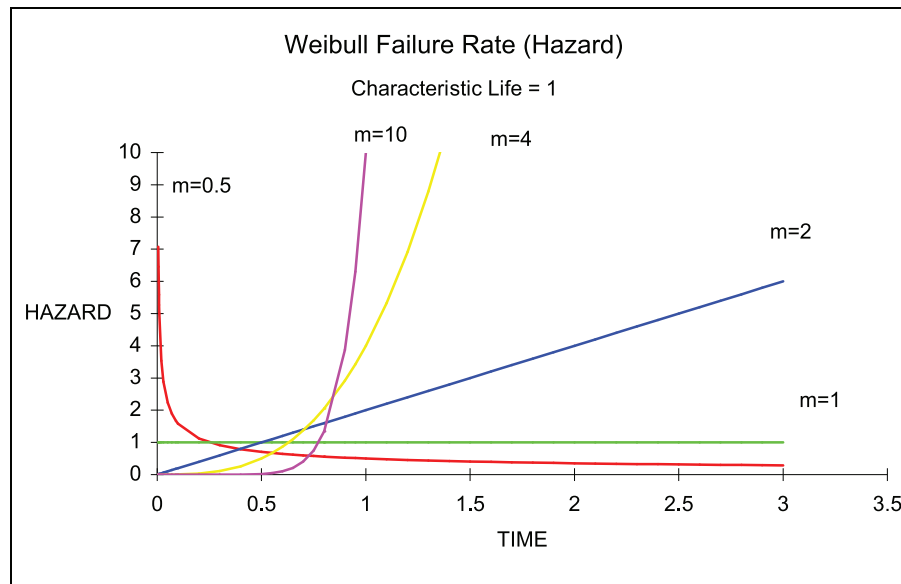


Figure 4.2 Weibull Distribution



4.3 Calculations of Failure Rates

To estimate field failure rates from reliability studies, many factors must be considered. One primary requirement is the identification of individual failure mechanisms in order to ascribe the failures to the proper categories used in the Spansion reliability model.

4.3.1 Considerations and Assumptions

1. Defective subpopulations and Early Life failures:

In any production lot a defective subpopulation may exist. These are devices that fail by a mechanism that is not common to the general population and is usually the result of some processing error or defect. These failures usually occurs early and consequently called Early Life failures. For the purposes of the Reliability Report Early Life is defined as 4,000 field equivalent hours (FEH) - actual life test hours multiplied by the acceleration factor for the mechanism.

The early life failure rate will be reported in FITs (failures per billion unit-hours).

2. Inherent Life failures:

Failures that occur in excess of 4,000 equivalent field hours are usually caused by mechanisms related to defects that could occur in any product of this type. These are known here as Inherent Life failures. If the first read-time in a life test is equivalent to or greater than 4,000 hours for a given mechanism, the data will be considered IL data, and unless there is no failure at this time, it will be considered that no data exists for this mechanism for Early Life. If this first read time has zero failures, Early Life will be calculated at 4,000 hours assuming no failures.

3. Estimation of thermal acceleration factors:

The best-known activation energies for each mechanism are used in calculating the thermal acceleration using the standard Arrhenius equation for thermal acceleration. For each process group/package combination, representative acceleration factors were estimated based on the weighted average of acceleration factors of individual devices in that group.

4. Voltage acceleration:

Certain failure mechanisms are accelerated by voltage stresses above normal operating voltage. The formula for voltage acceleration is shown below:

$$VAF = \exp\left[\left\{ \frac{230 \gamma (V_s - V_n)}{T_{ox}} \right\}\right]$$

VAF is the voltage acceleration factor, **V_s** is the test voltage, **V_n** is the nominal operating voltage, **T_{ox}** is the oxide thickness in Å, and gamma (γ) is a constant of value "3" for oxide defect related mechanisms and 1 for intrinsic oxide related ones.

For charge gain (floating gate devices), VAF varies just as the exponential of the voltage difference.

5. It is common in reliability literature to see failure rates stated at a specified level of confidence:

For example, a 60% upper confidence limit on the failure rate indicates that unless a 4 in 10 chance (40%) has occurred, the true population failure rate is less than the stated limit. The summation of individual failure rate components, each at 60% confidence, will however, result in an overall failure rate at an unknown confidence level that may dramatically exceed 60%.

The failure rates quoted in the Quarterly Reliability Report are at a 60% upper confidence level.

5. Data Summaries by Product Families

Product Family	Process Technology	Section/Page
Am29BD-H	CS 69, CS 69L	Section 6.4 on page 16
Am29BL-C	CS 39S, CS 39LS	Section 6.1 on page 13
Am29DL-B	CS 39S, CS 39LS	Section 6.1 on page 13
AM29DL-H	CS 69, CS 69L	Section 6.4 on page 16
Am29F-B	CS 39S, CS 39LS	Section 6.1 on page 13
Am29F-D	CS 49S	Section 6.2 on page 14
Am29LV-B	CS 39S, CS 39LS	Section 6.1 on page 13
Am29LV-D	CS 49S	Section 6.2 on page 14
Am29SL-C	CS 39S, CS 39LS	Section 6.1 on page 13
Am29SL-D	CS 49S	Section 6.2 on page 14
S19FL-P	CS 129, CS 129L, CS 129AL	Section 6.8 on page 20
S25FL-P	CS 129, CS 129L, CS 129AL	Section 6.8 on page 20
S25FL-S	CS 239LS	Section 6.10 on page 22
S29AL-D	CS 49SS	Section 6.3 on page 15
S29AL-J	CS 69SS, CS 69LSS	Section 6.6 on page 18
S29AS-J	CS 69SS, CS 69LSS	Section 6.6 on page 18
S29CD-J	CS 69SS, CS 69LSS	Section 6.6 on page 18
S29CL-J	CS 69S, CS 69LS	Section 6.6 on page 18
S29GL-N	CS 119S, CS 119LS	Section 6.7 on page 19
S29GL-P	CS 129, CS 129L, CS 129AL	Section 6.8 on page 20
S29GL-S	CS 239LS	Section 6.10 on page 22
S29JL-H	CS 69, CS 69L	Section 6.4 on page 16
S29JL-J	CS 69SS, CS 69LSS	Section 6.6 on page 18
S29NS-J	CS 69S, CS 69LS	Section 6.5 on page 17
S29NS-N	CS 119S, CS 119LS	Section 6.7 on page 19
S29NS-P	CS 129, CS 129L, CS 129AL	Section 6.8 on page 20
S29NS-R	CS 239, CS 239L	Section 6.9 on page 21
S29PL-J	CS 69S, CS 69LS	Section 6.5 on page 17
S29PL-N	CS 119S, CS 119LS	Section 6.7 on page 19
S29VS-R	CS 239, CS 239L	Section 6.9 on page 21
S29WS-N	CS 119S, CS 119LS	Section 6.7 on page 19
S29WS-P	CS 129, CS 129L, CS 129AL	Section 6.8 on page 20
S29WS-R	CS 239, CS 239L	Section 6.9 on page 21
S70FL-P	CS 129, CS 129L, CS 129AL	Section 6.8 on page 20
S70GL-P	CS 129, CS 129L, CS 129AL	Section 6.8 on page 20
S70PL-N	CS 119S, CS 119LS	Section 6.7 on page 19
S71GL-N	CS 119S, CS 119LS	Section 6.7 on page 19
S71GL-P	CS 129, CS 129L, CS 129AL	Section 6.8 on page 20
S71NS-J	CS 69SS, CS 69LSS	Section 6.6 on page 18
S71NS-N	CS 119S, CS 119LS	Section 6.7 on page 19
S71NS-P	CS 129, CS 129L, CS 129AL	Section 6.8 on page 20
S71NS-R	CS 239, CS 239L	Section 6.9 on page 21
S71PL-J	CS 69SS, CS 69LSS	Section 6.6 on page 18
S71PL-N	CS 119S, CS 119LS	Section 6.7 on page 19

Product Family	Process Technology	Section/Page
S71VS-R	CS 239, CS 239L	Section 6.9 on page 21
S71WS-N	CS 119S, CS 119LS	Section 6.7 on page 19
S71WS-P	CS 129, CS 129L, CS 129AL	Section 6.8 on page 20
S71WS-R	CS 239, CS 239L	Section 6.9 on page 21
S72NS-P	CS 129, CS 129L, CS 129AL	Section 6.8 on page 20
S72NS-R	CS 239, CS 239L	Section 6.9 on page 21
S72VS-R	CS 239, CS 239L	Section 6.9 on page 21
S72WS-R	CS 239, CS 239L	Section 6.9 on page 21
S72XS-R	CS 239, CS 239L	Section 6.9 on page 21
S98WS-R	CS 239, CS 239L	Section 6.9 on page 21

6. Data Summaries by Process Technology

6.1 Am29BL-C, Am29DL-B, Am29F-B, Am29LV-B, Am29SL-C Product Families CS 39S, CS 39LS

This 0.32 micron CMOS Flash technology was introduced in April 1998 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are double metal with contact plugs and barrier metal.

CS 39S, CS 39LS

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Points / Test Results				Modeling Parameters @ 55°C					Average Failure Rate FITS @ 55°C, 60% Conf.	
	24 hrs	168 hrs	1,000 hrs	2,000 hrs	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life	Inherent Life
PLASTIC											
Sample Size	8888	8348	1680	100							
Zero fails, Process ave. Ea	0 (1)	0	0	0	0.66	150	1	150		26	2
Totals	0	0	0	0					54440	26	2

Note

1. Contributes to Early Life FITS.

CS 39S, CS 39LS

Data Retention Bake - 150°C

Reliability Stress	Number of Rejects	Sample Size	Failure Rate%	Failure Mechanism
500 hrs	0	2794	0.00	No Failures
1000 hrs	0	2874	0.00	No Failures
2000 hrs	0	2542	0.00	No Failures

6.2 Am29F-D, AmLV-D, AmSL-D Product Families CS 49S

This 0.23 micron CMOS Flash technology was introduced in June 1999 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are three metal layers with contact plugs and barrier metal.

CS 49S

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Points / Test Results				Modeling Parameters @ 55°C					Average Failure Rate FITS @ 55°C, 60% Conf.	
	24 hrs	168 hrs	1,000 hrs	2,000 hrs	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life	Inherent Life
PLASTIC											
Sample Size	4200	4192	1053	150							
Zero fails, Process ave. Ea	0 (1)	0	0	0	0.66	148	1	148		55	4
Totals	0	0	0	0					31909	55	4

Note

1. Contributes to Early Life FITS.

CS 49S

Data Retention Bake - 150°C

Reliability Stress	Number of Rejects	Sample Size	Failure Rate%	Failure Mechanism
500 hrs	0	1622	0.00	No Failures
1000 hrs	0	1472	0.00	No Failures
2000 hrs	0	1061	0.00	No Failures

6.3 S29AL-D Product Families CS 49SS

This 0.20 micron CMOS Flash technology was introduced in September 2004 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are three metal layers with contact plugs and barrier metal.

CS 49SS Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Points / Test Results				Modeling Parameters @ 55°C					Average Failure Rate FITS @ 55°C, 60% Conf.	
	24 hrs	168 hrs	1,000 hrs	2,000 hrs	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life	Inherent Life
PLASTIC											
Sample Size	7350	7347	1360	240							
Zero fails, Process ave. Ea	0 (1)	0	0	0	0.66	134	1	134		31	3
Totals	0	0	0	0					43503	31	3

Note

1. Contributes to Early Life FITS.

CS 49SS Data Retention Bake - 150°C

Reliability Stress	Number of Rejects	Sample Size	Failure Rate%	Failure Mechanism
500 hrs	0	1900	0.00	No Failures
1000 hrs	0	1900	0.00	No Failures
2000 hrs	0	877	0.00	No Failures

6.4 Am29BD-H, AM29DL-H, S29JL-H, Product Families CS 69, CS 69L

This 0.13 micron CMOS Flash technology was introduced in April 2003 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are three metal layers with contact plugs and barrier metal.

CS 69, CS 69L

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Points / Test Results				Modeling Parameters @ 55°C					Average Failure Rate FITS @ 55°C, 60% Conf.	
	24 hrs	168 hrs	1,000 hrs	2,000 hrs	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life	Inherent Life
PLASTIC											
Sample Size	7200	9199	2880	486							
Zero fails, Process ave. Ea	0 (1)	0	0	0	0.66	149	1	149		31	1
Totals	0	0	0	0					81299	31	1

Note

1. Contributes to Early Life FITS.

CS 69, CS 69L

Data Retention Bake - 150°C

Reliability Stress	Number of Rejects	Sample Size	Failure Rate%	Failure Mechanism
500 hrs	0	1800	0.00	No Failures
1000 hrs	0	2049	0.00	No Failures
2000 hrs	0	700	0.00	No Failures

6.5 S29CD-J, S29NS-J, S29PL-J, S71NS-J, S71PL-J Product Families CS 69S, CS 69LS

This 0.11 micron CMOS Flash technology was introduced in December 2003 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are three metal layers with contact plugs and barrier metal.

CS 69S, CS 69LS

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Points / Test Results				Modeling Parameters @ 55°C					Average Failure Rate FITS @ 55°C, 60% Conf.	
	24 hrs	168 hrs	1,000 hrs	2,000 hrs	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life	Inherent Life
PLASTIC											
Sample Size	10778	10653	2340	165							
Zero fails, Process ave. Ea	0 (1)	0	0	0	0.66	140	1	140		21	2
Totals	0	0	0	0					68103	21	2

Note

1. Contributes to Early Life FITS.

CS 69S, CS 69LS

Data Retention Bake - 150°C

Reliability Stress	Number of Rejects	Sample Size	Failure Rate%	Failure Mechanism
500 hrs	0	4636	0.00	No Failures
1000 hrs	0	4710	0.00	No Failures
2000 hrs	0	5120	0.00	No Failures

6.6 S29AL-J, S29AS-J, S29JL-J Product Families CS 69SS, CS 69LSS

This 0.11 micron CMOS Flash technology was introduced in February 2008 and utilizes a tunnel oxide, polysilicon floating gate, silicided poly word line and interconnections are three metal layers with contact plugs and barrier metal.

CS 69SS, CS69LSS

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 150°C

Failure Mechanisms	Read Points / Test Results				Modeling Parameters @ 55°C					Average Failure Rate FITS @ 55°C, 60% Conf.	
	24 hrs	168 hrs	1,000 hrs	2,000 hrs	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life	Inherent Life
PLASTIC											
Sample Size	5800	6599	1350	160							
Zero fails, Process ave. Ea	0 (1)	0	0	0	0.66	166	1	166		38	2
Totals	0	0	0	0					49069	38	2

Note

1. Contributes to Early Life FITS.

CS 69SS, CS69LSS

Data Retention Bake - 150°C

Reliability Stress	Number of Rejects	Sample Size	Failure Rate%	Failure Mechanism
500 hrs	0	2198	0.00	No Failures
1000 hrs	0	1900	0.00	No Failures
2000 hrs	0	700	0.00	No Failures

**6.7 S29GL-N, S29NS-N, S29PL-N, S29WS-N, S70PL-N, S71GL-N, S71NS-N, S71PL-N, S71WS-N Product Families
CS 119S, CS 119LS**

This 0.11 micron CMOS Flash technology was introduced in June 2004 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are three or four metal layers with contact plugs and barrier metal.

**CS 119S, CS 119LS
Data Summary and Failure Rate Estimation using Exponential Model
HTOL Stress Temperature - 150°C**

Failure Mechanisms	Read Points / Test Results				Modeling Parameters @ 55°C					Average Failure Rate FITS @ 55°C, 60% Conf.	
	24 hrs	168 hrs	1,000 hrs	2,000 hrs	Ea eV	TAF	VAE	OAF	MTTF (yrs)	Early Life	Inherent Life
PLASTIC											
Sample Size	10150	11246	1930	200							
Zero fails, Process ave. Ea	0 (1)	0	0	0	0.66	130	1	130		22	2
Totals	0	0	0	0					59419	22	2

Note

1. Contributes to Early Life FITS.

**CS 119S, CS 119LS
Data Retention Bake - 150°C**

Reliability Stress	Number of Rejects	Sample Size	Failure Rate%	Failure Mechanism
500 hrs	0	2881	0.00	No Failures
1000 hrs	0	2753	0.00	No Failures

**6.8 S19FL-P, S25FL-P, S29GL-P, S29NS-P, S29WS-P, S70FL-P, S70GL-P, S71GL-P, S71NS-P, S71WS-P, S72NS-P Product Families
CS 129, CS 129L, CS 129AL**

This 90 nanometer CMOS Flash technology was introduced in Aug 2006 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are three copper layers.

CS 129, CS 129L, CS 129AL

**Data Summary and Failure Rate Estimation using Exponential Model
HTOL Stress Temperature - 150°C**

Failure Mechanisms	Read Points / Test Results				Modeling Parameters @ 55°C					Average Failure Rate FITS @ 55°C, 60% Conf.	
	24 hrs	168 hrs	1,000 hrs	2,000 hrs	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life	Inherent Life
PLASTIC											
Sample Size	11314	13500	2350	150							
Zero fails, Process ave. Ea	0 (1)	0	0	0	0.66	145	1	145		19	1
Totals	0	0	0	0					78503	19	1

Note

1. Contributes to Early Life FITS.

CS 129, CS 129L, CS 129AL

Data Retention Bake - 150°C

Reliability Stress	Number of Rejects	Sample Size	Failure Rate%	Failure Mechanism
500 hrs	0	3607	0.00	No Failures
1000 hrs	0	3910	0.00	No Failures

**6.9 S29NS-R, S29VS-R, S29WS-R, S71NS-R, S71VS-R, S71WS-R, S72NS-R, S72VS-R, S72WS-R, S72XS-R, S98WS-R Product Families
CS 239, CS 239L**

This 65 nanometer CMOS Flash technology was introduced in September 2007 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are three copper layers.

CS 239, CS 239L

**Data Summary and Failure Rate Estimation using Exponential Model
HTOL Stress Temperature - 125°C**

Failure Mechanisms	Read Points / Test Results				Modeling Parameters @ 55°C					Average Failure Rate FITS @ 55°C, 60% Conf.	
	24 hrs	168 hrs	1,000 hrs	2,000 hrs	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life	Inherent Life
PLASTIC											
Sample Size	4302	4300	690	150							
Zero fails, Process ave. Ea	0 (1)	0	0	0	0.66	41	1	41		53	15
Totals	0	0	0	0					7389	53	15

Note

1. Contributes to Early Life FITS.

CS 239, CS 239L

Data Retention Bake - 150°C

Reliability Stress	Number of Rejects	Sample Size	Failure Rate%	Failure Mechanism
500 hrs	0	1450	0.00	No Failures
1000 hrs	0	1446	0.00	No Failures

6.10 S29GL-S, S25FL-S Product Families CS 239LS

This 65 nm Mirror bit flash technology was introduced in September 2010 and utilizes a tunnel oxide, Silicon Nitride (SiN) data storage layer, silicided poly word line and interconnections are four metal layers with contact plugs and barrier metal.

CS 239LS

Data Summary and Failure Rate Estimation using Exponential Model HTOL Stress Temperature - 125°C

Failure Mechanisms	Read Points / Test Results				Modeling Parameters @ 55°C					Average Failure Rate FITS @ 55°C, 60% Conf.	
	24 hrs	168 hrs	1,000 hrs	2,000 hrs	Ea eV	TAF	VAF	OAF	MTTF (yrs)	Early Life	Inherent Life
PLASTIC											
Sample Size	2075	3025	445	50							
Zero fails, Process ave. Ea	0 (1)	0	0	0	0.66	53	1	53		83	19
Totals	0	0	0						5980	83	19

Note

1. Contributes to Early Life FITS.

CS 239LS

Data Retention Bake - 150°C

Reliability Stress	Number of Rejects	Sample Size	Failure Rate%	Failure Mechanism
500 hrs	0	300	0.00	No Failures
1000 hrs	0	300	0.00	No Failures

7. Data Summaries by Package Family

7.1 FBGA (Fine Pitch Ball Grid Array Package)

Reliability Stress		Number of Rejects	Sample Size	Failure Rate PPM	Failure Mechanism
Temperature Cycle	100 cycles	0	3062	0	No Failures
	1000 cycles	0	3215	0	No Failures
Unbiased HAST	96 hrs	0	3062	0	No Failures
HAST	264 hrs	0	2058	0	No Failures

7.2 MCP (Multi-Chip Fine Pitch Ball Grid Array Package)

Reliability Stress		Number of Rejects	Sample Size	Failure Rate PPM	Failure Mechanism
Temperature Cycle	100 cycles	0	65	0	No Failures
	300 cycles	0	40	0	No Failures
	500 cycles	0	847	0	No Failures
	1000 cycles	0	847	0	No Failures
Unbiased HAST	96 hrs	0	912	0	No Failures
HAST	264 hrs	0	385	0	No Failures

7.3 TSOP (Thin Small Outline Package)

Reliability Stress		Number of Rejects	Sample Size	Failure Rate PPM	Failure Mechanism
Temperature Cycle	100 cycles	0	3465	0	No Failures
	1000 cycles	0	3926	0	No Failures
Unbiased HAST	96 hrs	0	3471	0	No Failures
HAST	96 hrs	0	3471	0	No Failures

7.4 SOIC (Small Outline Integrated Circuit)

Reliability Stress		Number of Rejects	Sample Size	Failure Rate PPM	Failure Mechanism
Temperature Cycle	100 cycles	0	3003	0	No Failures
	500 cycles	0	1179	0	No Failures
	1000 cycles	0	4025	0	No Failures
Unbiased HAST	96 hrs	0	4182	0	No Failures
HAST	96 hrs	0	3003	0	No Failures

7.5 PLCC (Plastic Leaded Chip Carrier)

Reliability Stress		Number of Rejects	Sample Size	Failure Rate PPM	Failure Mechanism
Temperature Cycle	100 cycles	0	1155	0	No Failures
	1000 cycles	0	1231	0	No Failures
Unbiased HAST	96 hrs	0	1155	0	No Failures
HAST	96 hrs	0	924	0	No Failures

7.6 PQFP (Plastic Quad Flat Package)

Reliability Stress		Number of Rejects	Sample Size	Failure Rate PPM	Failure Mechanism
Temperature Cycle	100 cycles	0	1233	0	No Failures
	1000 cycles	0	1233	0	No Failures
Unbiased HAST	96 hrs	0	1233	0	No Failures
HAST	96 hrs	0	1233	0	No Failures

7.7 PDIP (Plastic Dual Inline Package)

Reliability Stress		Number of Rejects	Sample Size	Failure Rate PPM	Failure Mechanism
Temperature Cycle	100 cycles	0	77	0	No Failures
	1000 cycles	0	77	0	No Failures
HAST	96 hrs	0	77	0	No Failures

7.8 SSOP (Shrink Small Outline Package)

Reliability Stress		Number of Rejects	Sample Size	Failure Rate PPM	Failure Mechanism
Temperature Cycle	100 cycles	0	77	0	No Failures
	1000 cycles	0	77	0	No Failures
Unbiased HAST	96 hrs	0	77	0	No Failures
HAST	96 hrs	0	77	0	No Failures

7.9 WSON/USON (Small Outline No Lead Package/Ultra Thin Small Outline No Lead Package)

Reliability Stress		Number of Rejects	Sample Size	Failure Rate PPM	Failure Mechanism
Temperature Cycle	100 cycles	0	1540	0	No Failures
	1000 cycles	0	1463	0	No Failures
Unbiased HAST	96 hrs	0	1540	0	No Failures
HAST	96 hrs	0	385	0	No Failures

8. Appendix

Reference Publications

1. *Quality and Reliability for the 1990's* Pub. Ref. No. 09581B
2. *Wafer Level Reliability Program for the 1990's* Pub. Ref. No. 17688A
3. *Packaging: Packages and Packing Methodologies* Pub. Ref. No. 12019C
4. *P.A. Tobias and D.C. Trindade, Applied Reliability,* Van Nostrand Reinhold Co., New York, 1986
5. *JEP122D, Failure Mechanisms and Models for Semiconductor Devices,* October 2008
6. *Reliability Physics and Engineering, Time-To-Failure Modeling,* McPherson, J.W. 2010
7. *Method for Calculating Failure Rates in Units of FITs,* JESD85, JUL 2001
8. *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms,* JESD91-A, AUG 2003

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