

## Spansion leverages its flexible fab strategy and chip architecture

*By Debra Vogler, Senior Technical Editor  
April 10, 2008*

**Apr. 10, 2008 - Pure-play flash memory provider Spansion Inc. says it is now sampling 65nm MirrorBit Eclipse flash memory technology for wireless handsets to strategic OEM customers, with volume production planned for 2H08 at the company's new flagship 300mm SP1 fab in Japan.**

According to John Nation, director of corporate marketing at Spansion, the plan is to do 45nm sampling late this year and ramp those products sometime in 2009. (Spansion had indicated other 65nm and 45nm MirrorBit work planned for SP1 in a recent interview with WaferNEWS, but has since indicated the 45nm ramp will be pushed out to next year.)

"The MirrorBit Eclipse architecture offers higher performance and is particularly suitable for combined code storage and execution and data storage applications," Nation explained to WaferNEWS, making it "an ideal solution for wireless handsets, which is a large segment of the NOR marketplace." An architectural feature of the chip is the use of a programmable microcontroller to manage the flash memory cell, which "makes it more manufacturable and reduces costs," he noted. The Eclipse also enables code and data storage on the same die, resulting in improved performance such as high-speed programming, low power, high density, and fast application switching.

An added advantage of using a programmable microcontroller is that it is also used for built-in self-test (BIST), which reduces overall test costs (particularly in the back-end) "because you can do wafer-level testing using BIST," said Nation. Using BIST the test times are the same for a 300mm wafer as for a 200mm wafer, but on 300mm "you're going to be testing somewhere between 2.2x-2.4x the number of die", he explained, and the company anticipates this to be a significant cost benefit going forward.

Spansion is heavily committed to using immersion lithography at 65nm to manufacture its MirrorBit technology and beyond, making significant investments in immersion even during a time of market softness. The company views the choice of immersion in combination with 300mm wafer manufacturing as a way to offer aggressive roadmaps to its customers. "There's significant jeopardy in terms of how one would scale to 45nm if you only have 200mm equipment," said Nation.

Nation told WaferNEWS that another reason to choose immersion lithography now is that it fits well with Spansion's flexible manufacturing strategy. "We have our own internal fabs, but also external foundries," he said. The company is currently using TSMC at 90nm, and toward the end of this year will be ramping 65nm at SMIC. "So another part of the story here is to have the flexibility to be able to switch manufacturing between our different fabs and external foundries. You look at the foundries' decisions...they're building leading-edge manufacturing facilities, so immersion was the more attractive option." -- D.V.