

Am29BDS323D: Ultra Performance Flash

Application Note



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Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal documentation improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

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AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

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Am29BDS323D: Ultra Performance Flash

Application Note

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The Am29BDS323D burst mode flash memory device represents AMD's unique solution to the customer's high performance, low voltage needs. The Am29BDS323D is a 32 Mbit, 1.8 Volt-only, simultaneous Read/Write, Burst Mode Flash memory device, organized as 2,097,152 words of 16 bits each. It provides burst read access times as fast as 20 ns, while being able to simultaneously perform program or erase operations.

The Am29BDS323D key distinctive characteristics include:

- 20 ns synchronous burst access time
- 120 ns synchronous initial access time
- 90 ns asynchronous access time
- Multiplexed data/addressing signals
- Programmable Wait States
- Power Saving Function
- Dual Operations – reading simultaneously with program or erase operations
- Single power supply between 1.7 V–1.9 V

Using this device can drastically improve system performance, reduce cost, and lower overall power consumption. This device is ideal for the cellular and portable markets.

Burst Read Access

The Am29BDS323D provides sequential read accesses as fast as 20 ns for each word. Each non-sequential (or random) access begins with a slower initial read access, which may be followed by an unlimited number of much faster sequential read accesses. Only the address for the initial non-sequential read must be provided to the memory; an internal address counter provides sequential addresses.

Multiplexed Address and Data Signals

The Am29BDS323D has multiplexed address and data functions on the same set of pins. The lower 16 bits of the address bus (A0–A15) are shared with the data bus, DQ0–DQ15. This reduces the memory pin count.

Burst Mode Control Signals

In addition to conventional Flash I/O, address and control signals, the Am29BDS323D device requires the following Burst specific functions: Address Valid and a Clock.

Address Valid (AVD#)

AVD# Low indicates that a valid address is present on the address inputs and causes the address to be loaded into an internal address counter at the next rising edge of Clock. It also opens an address latch and starts a memory access. When AVD# goes High, the address is latched and the address lines may then be used as data outputs for the read operation. AVD# High ignores subsequent address inputs.

Clock (CLK)

Clock input can be tied to the system or clock and provides the fundamental timing and internal operating frequency. Care should be taken to ensure proper phase relationship between clock connected to the Flash devices and the clock used by the processor.

CLK, used in conjunction with AVD#, latches address input and initiates the burst mode operation. The AVD# goes high and must stay high for the data operation. After the initial word is read, subsequent rising edges of CLK increment the internal address counter.

Burst Read Operation

Am29BDS323D has two different read modes: Non-Burst and Burst Read.

Non-Burst read is an asynchronous operation. To read data from the memory array, the system must first assert a valid address on A/DQ0–A/DQ15 and A16–A21, while driving AVD# and CE# to V_{IL} . WE# and OE# should remain at V_{IH} . Note that CLK must remain low for asynchronous read operations. The rising edge of AVD# latches the address, after which the system can drive OE# to V_{IL} . The data will appear on A/DQ0–A/DQ15 following the asynchronous access delay. The internal state machine is set for reading array data upon device power-up, or after a hardware reset.

Burst read is a synchronous operation and requires two command sequences after power up in order to proceed with the burst operation. They are Set Wait Count

command sequence and Enable PS Mode command sequence.

The Set Wait Count command sequence instructs the device to set a particular number of clocks for the initial access in burst mode. Set Wait Count defaults to the maximum seven cycles wait state setting. The Enable PS (Power Saving) Mode command sequence is required to set the device to the PS Mode. The PS Mode (Power Saving Mode) reduces the number of DQ outputs switching to save power. These two command sequences are only needed during the initial power up. After that user can do burst read as many times as needed without having to perform Set Wait State and Power Saving command sequences. During initial power up the PS function is disabled.

When the device first powers up, it is enabled for asynchronous read operation. The device will automatically be enabled for burst mode on the first rising edge on the CLK input, while AVD# is held low. Prior to activating the clock signal, the system should determine how many wait states are required for the initial word of

each burst sequence. The system would then write the Set Wait Count command sequence. The wait state command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The system may optionally activate the PS mode (see “Power Saving Mode”) by writing the Enable PS Mode command sequence at this time, but note that the PS mode can only be disabled by a hardware reset or power-up/power-down. The device is capable of continuous, sequential (linear) burst operation. The device will continue to output sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location, until the system asserts CE# High, RESET# Low, or AVD# Low in conjunction with a new address. For all the conditions of burst read, including wait states during the burst read refer to the data sheet.

RDY indicates the status of the Burst read. When RDY is low it means the data is not ready. RDY high specifies that this data is valid.

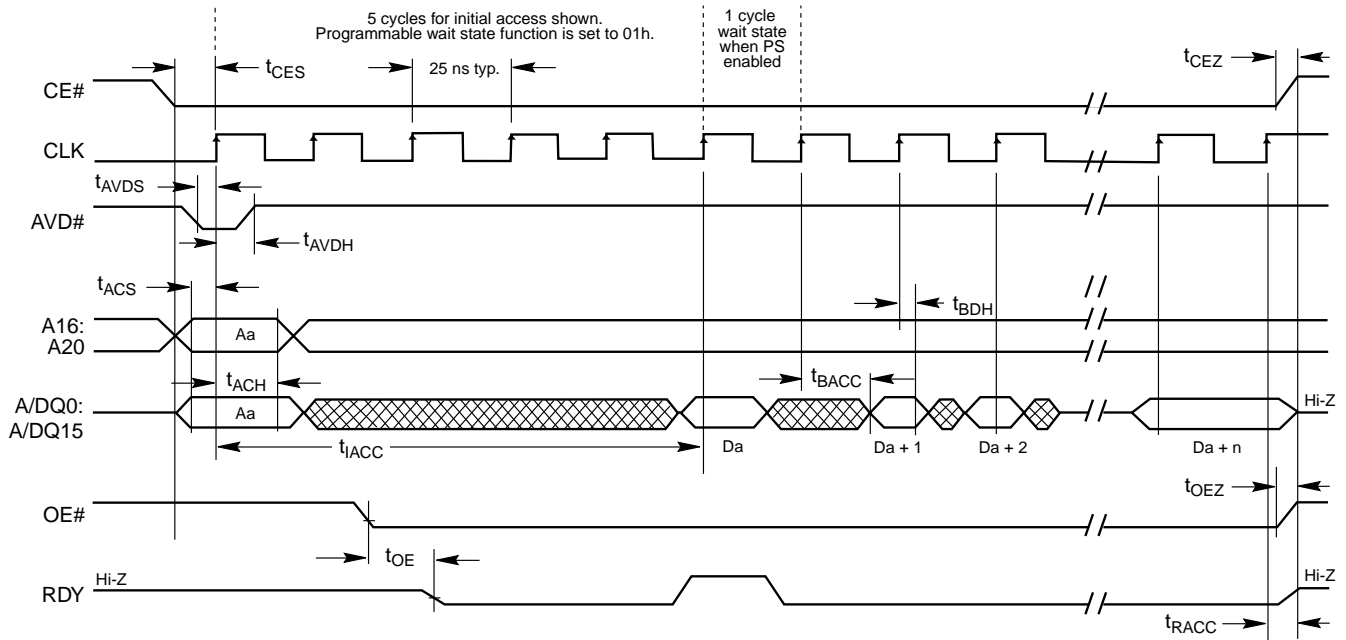


Figure 1. Timing Diagram for the Am29BDS323 Burst Mode Read

Figure 1 illustrates the timing diagram for a burst access read. The starting burst address is loaded during the rising edge of the CLK following AVD# going low.

System Performance Impact

The first random read has an access time of 120 ns, while sequential reads have an access time of 20 ns. A

comparison between Non-Burst Mode and Burst Mode in Table 1 clearly illustrates the reduction in access time. For a 40 MHz burst (25 ns CLK cycle time), the data must be ready no later than 20 ns after the CLK edge to allow a 5 ns data hold time.

Example 1

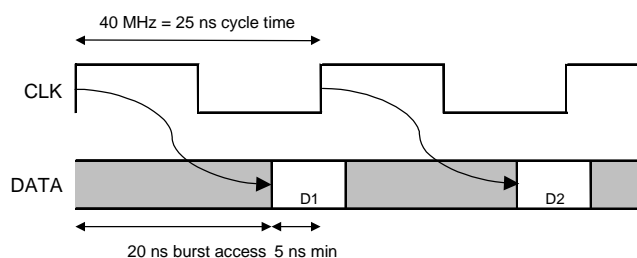


Table 1. Comparing Read Times Between Non-Burst and Burst Mode

	Non-Burst Asynchronous	Burst Mode Synchronous
Byte 0	90 ns (t_{ACC})	120 ns (t_{ACC})
Byte 1	90 ns	25 ns
Byte 2	90 ns	25 ns
Byte 3	90 ns	25 ns
Byte 4	90 ns	25 ns
Byte 5	90 ns	25 ns
Byte 6	90 ns	25 ns
Byte 7	90 ns	25 ns
Total Flash Access Time	720 ns	295 ns

Example 2

The following are calculations for Table 2. This example shows a comparison between Non-Burst and Burst Mode at the system level.

Depending on the system delay and system clocks, the user can achieve different levels of system performance.

Assuming:

System clock speed = 30 MHz, $t_{CLK} = 1/30 = 33$ ns

System delay = 8 ns (consisting of 5 ns data hold time and 3 ns setup and other delay)

For Non-Burst (Asynchronous):

$$\begin{aligned}
 t_{SYSACC} &= t_{ACC} + t_{HOLDTIME} + t_{SETUP} \\
 &= 90 \text{ ns} + 5 \text{ ns} + 3 \text{ ns} \\
 &= 98 \text{ ns}
 \end{aligned}$$

3 clock cycles will be required

For Burst Mode (Synchronous):

$$t_{ACC} = 120 \text{ ns}$$

$$\begin{aligned}
 t_{SYSACC} &= t_{ACC} + t_{HOLDTIME} + t_{SETUP} \\
 &= 120 \text{ ns} + 5 \text{ ns} + 3 \text{ ns} \\
 &= 128 \text{ ns}
 \end{aligned}$$

4 clock cycles will be required

$$t_{ACC} = 25 \text{ ns}$$

$$\begin{aligned}
 t_{SYSACC} &= t_{ACC} + t_{HOLDTIME} + t_{SETUP} \\
 &= 25 \text{ ns} + 5 \text{ ns} + 3 \text{ ns} \\
 &= 33 \text{ ns}
 \end{aligned}$$

Exactly 1 clock cycle will be required

Table 2. Comparing Read Times Between Non-Burst and Burst Mode

	Non-Burst Asynchronous		Burst Mode Synchronous	
	No. of Clock Cycles	Total Time	No. of Clock Cycles	Total Time
Byte 0	3	99 ns	4	132 ns
Byte 1	3	99 ns	1	33 ns
Byte 2	3	99 ns	1	33 ns
Byte 3	3	99 ns	1	33 ns
Byte 4	3	99 ns	1	33 ns
Byte 5	3	99 ns	1	33 ns
Byte 6	3	99 ns	1	33 ns
Byte 7	3	99 ns	1	33 ns
Total Time	24	792 ns	11	363 ns

Tables 1 and 2 show how much time is required to read eight consecutive bytes from memory in each mode.

These tables clearly illustrate that burst mode performs faster than non-burst mode. To achieve optimum performance from this device, the system's program should be structured such that the device can perform as many sequential reads as possible. The more code the system reads in a sequential, continuous fashion, the faster the average access time.

Programmable Wait States

The programmable wait state feature specifies the number of additional clock cycles that must pass after AVD# is driven active before the first data will be available. This feature adds the appropriate number of wait states to match the total initial access cycles. Please refer to Table 3 and Figure 2 that show the set up for total initial access cycles. The wait state is programmed using a 3-cycle Embedded Command. On the last command, 555h must be entered on the lower-order addresses. The wait state defaults to the longest setting upon power up, but it is recommended to always input the wait state.

Table 3. Command Sequence For Total Initial Access Cycles

Command Sequence	Cycles	Bus Cycles						Total Initial Access Cycles
		First		Second		Third		
		Address	Data	Address	Data	Address	Data	
Set Wait State	3	555	AA	2AA	55	000555h	C0h	4
	3	555	AA	2AA	55	001555h	C0h	5
	3	555	AA	2AA	55	002555h	C0h	6
	3	555	AA	2AA	55	003555h	C0h	7

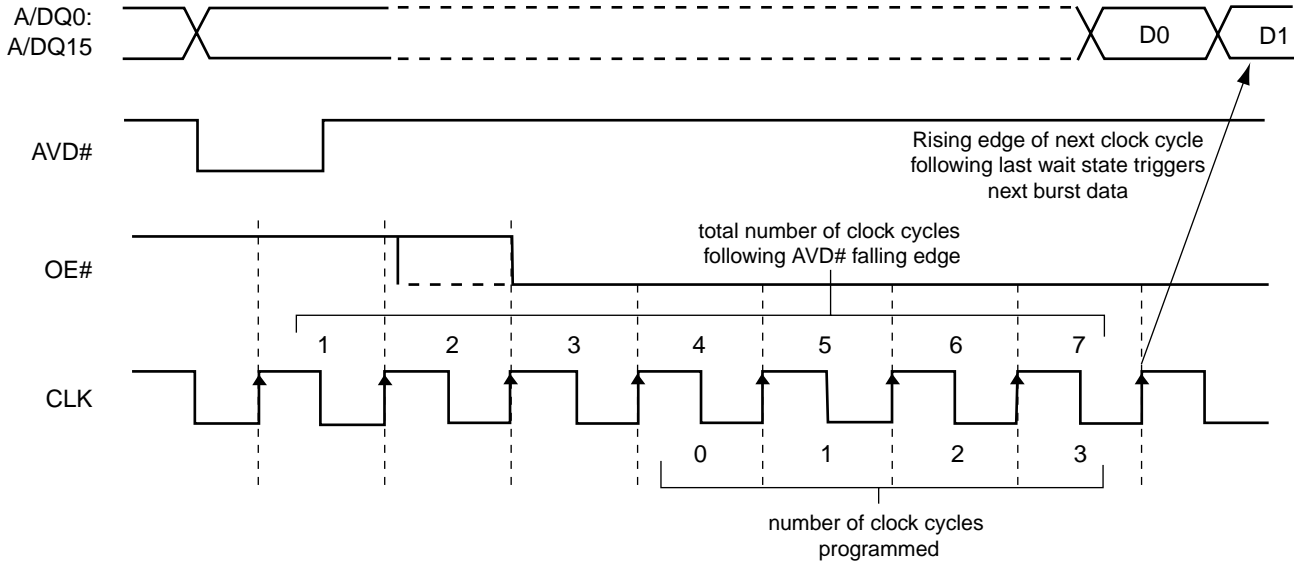


Figure 2. Total Initial Access Cycles Timing Diagram

Power Saving Mode

The Power Saving Mode reduces the amount of switching on the data output bus by changing the minimum number of bits possible, thereby reducing power consumption. This function is active only during burst mode operations.

Power Saving Mode is disabled as the default when the device powers up. Power savings Mode is enabled with a 3-cycle Embedded Command (Refer to the Command Definition Table in the data sheet). When Power Savings is enabled, the device needs one additional wait state during the start of burst. This is in addition to whatever wait state is programmed. The RDY# goes low during this extra CLK cycle.

During power savings bursts, the device compares the 16-bit word previously output to the system with the new word to be output. If the number of bits to be switched is 0–8 (less than half the bus width), the device simply outputs the new word on the data bus. However, the device inverts the data if the number of bits to be switched is 9 or higher. This reduces the number of outputs switching externally to save power, effectively reducing the number of transitions to eight. The device indicates to the system whether or not the data is inverted via the PS pin output. If the word on the data bus is not inverted, PS = V_{OL} = 0; if the word on the data bus is inverted, PS = V_{OH} = 1.

Example 3

Table 4. Power Savings Mode Example

Address	Memory Cell Data	No. of Bits Needed to be Switched w/o PS From Previous Address	No. of Bits Switched with PS	PS Output	DQ Outputs with PS
n	1111 1111 1111 1111	—	—	0	1111 1111 1111 1111
n+1	1111 1111 1111 1110	1	1	0	1111 1111 1111 1110
n+2	1111 1111 1111 1111	1	1	0	1111 1111 1111 1111
n+3	1111 0000 0000 0000	12	4	1	0000 1111 1111 1111
n+4	1111 0000 0000 0001	15	1	1	0000 1111 1111 1110
n+5	1111 1111 1111 1111	5	5	0	1111 1111 1111 1111
n+6	0000 0000 0000 0000	16	0	1	1111 1111 1111 1111

Power Saving Mode also reduces the total current by approximately 10% to 15%.

The example in Table 5 is based on a design engineer's assumptions of 40 MHz system clock speed, 40 pF load, with random data.

The actual savings depends heavily on customer data.

Table 5. Comparison of Power Consumption Between Without Power Saving Mode and With Power Saving Mode

	Without Power Saving	With Power Saving
Average Number of I/Os Switching	8	6
I_{CC} for internal operation	12 mA	12 mA
I_{CC} for 1 I/O to switch	2 mA	2 mA
Total I_{CC} for all I/O	16 mA	12 mA
Total Current	28 mA	24 mA
Power Consumption Saving	50.4 mW	43.2 mW

Conclusion

The Am29BDS323D Burst Mode flash memory device enables the designer to improve system performance. The programmable wait state feature allows the user more flexibility in changing the operating frequency.

The Power Saving Function helps reduce power consumption. The device consumes around 10% to 15% less power. The Am29BDS323D is the best solution for high performance systems that have the flexibility to integrate the required burst mode interface. It eliminates the need for external logic to generate wait states.